

Memory Roadmap Update & Industry Status

Pete MacWilliams

-Intel Fellow DPG

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Jon Kang

-Sr. V.P. Samsung Memory Div

Shozo Saito

-G.M. Memory Div, Toshiba

February 27, 2001

Memory Roadmap Update

Pete MacWilliams
Intel Fellow
Desktop Product Group
Intel Corporation

Agenda

- **Memory Strategy & Roadmap**
- **DDR Program Status**
- **RDRAM* Program Status**
- **Summary**

**Other names and brands are the property of their respective owners.*

Memory Strategy

- **New Memory Technologies primarily driven by Desktop and Server Platform Volumes**
 - Intel's Direction:
 - Desktop transitioning from SDRAM to RDRAM
 - Server transitioning from SDRAM to DDR
- **Mobile and Workstation Platforms do not typically drive New Memory Technologies**
 - Workstation segments typically share with either Server or Desktop platforms, with rapid adoption
 - Mobile segments typically share with desktop, but lag in time due to different power and performance requirements

No Fundamental Change to Intel Memory Strategy

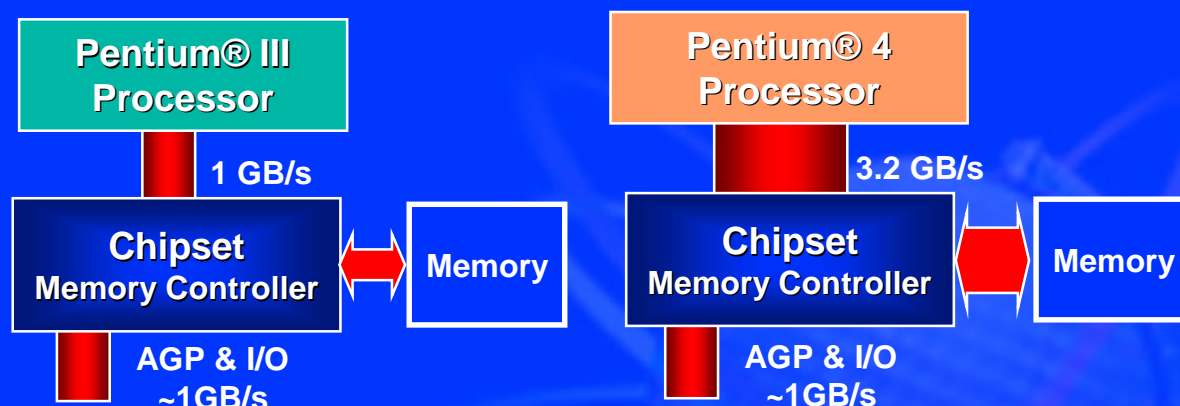
Memory Strategy (cont)

The Pentium® 4 Processor

- **RDRAM – “The best solution” (Now)**
 - Robust technology shipping in volume for >1 year
 - Pentium® 4 Processor will drive learning curve in ‘01
 - Best technology for the Intel Pentium™ 4 Processor Platform
 - Performance matched to processor bus
 - Best performance at a given platform cost
 - Memory pricing that limited ramp in ‘00 is coming down
 - Cost look competitive with alternatives
- **PC133 – “The lowest price solution” (2H/01)**
 - Good solution for applications with low bandwidth demands
 - Supports lower platform price points
- **DDR – “Another price/performance option” (1H/02)**

RDRAM Remains the Primary Desktop Memory Solution
Multiple Memory Technologies will be Supported

Balanced Platforms



Memory Type	Bandwidth*
1 Channel PC133	1.0 GB/s
1 Channel DDR200	1.6 GB/s
1 Channel RDRAM	1.6 GB/s
2 Channel PC133	2.0 GB/s
2 Channel DDR200	3.2 GB/s
2 Channel RDRAM	3.2 GB/s

All bandwidths shown are peak and do not account for workloads or efficiencies

Pentium® III Processor Platforms

- SDRAM (1 ch) is sufficient for systems with limited AGP & I/O traffic to memory

Pentium® 4 Processor Platforms

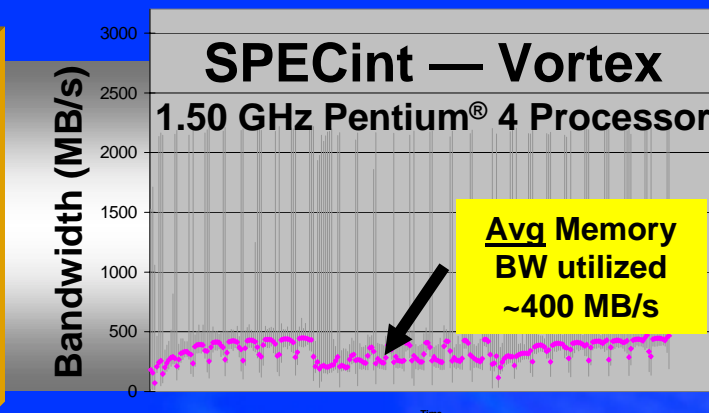
- Dual channel memory required to support bandwidth demanding apps
- System demands are application dependent

Dual Memory Channels

- Higher memory bandwidth requires higher system cost
- RDRAM is most efficient due to high bandwidth per pin

Measured Data Bandwidth on a Low-Demand Application

2-Ch
RDRAM

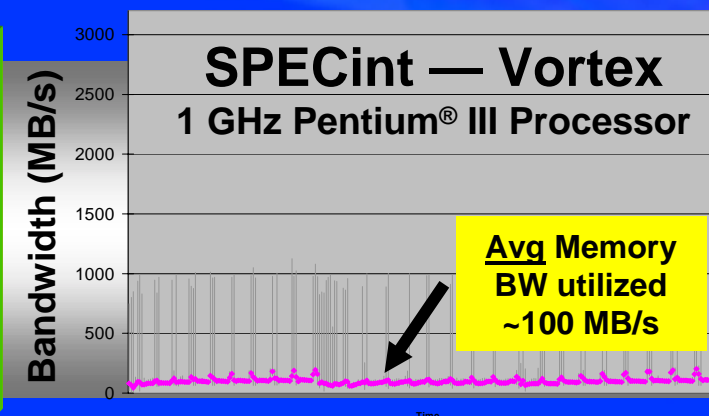


Intel®
850
Chipset

FSB



2-Ch
RDRAM



Intel®
840
Chipset

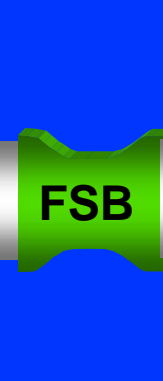
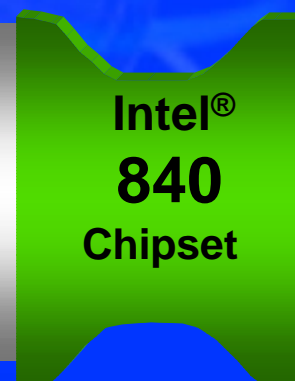
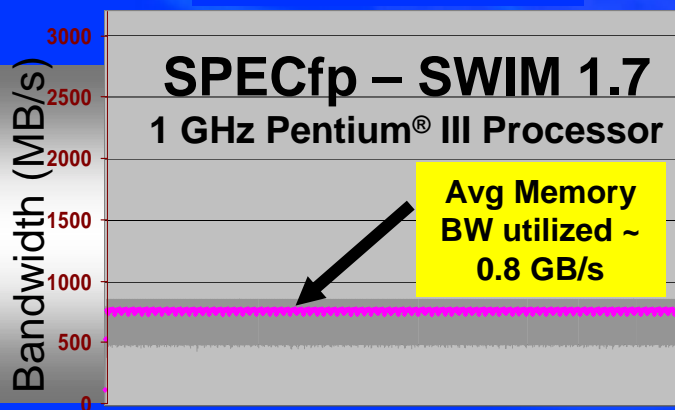
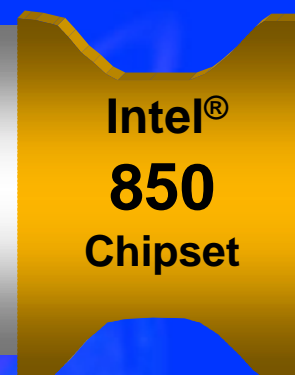
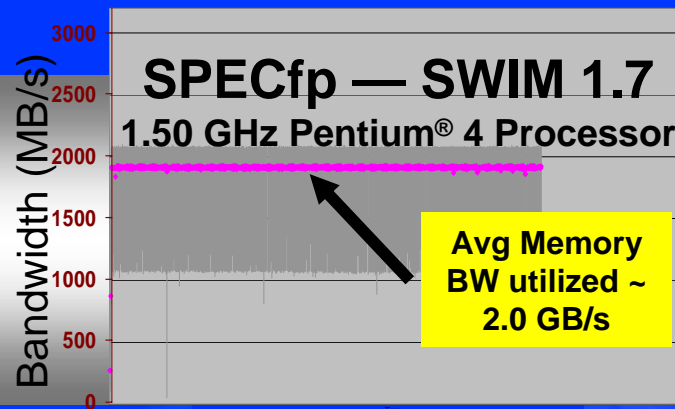
FSB



Some applications do not demand high memory bandwidth

Note: Vortex is a object oriented database benchmark

Measured Data Bandwidth on a Demanding Application



**High memory bandwidth with Intel® NetBurst™ Microarchitecture
can make a big difference**

Note: SWIM is a Shallow Water Modeling Benchmark

Platform Costs

- Current Dual Channel RDRAM platforms have cost adders
 - 6 layer boards, memory sockets, termination, etc.
- Dual Channel RDRAM Platform cost reductions in progress
 - OEMs are already starting to cost reduce 2 channel RDRAM boards

	<u>PC133</u>	<u>DDR</u>	<u>RDRAM</u>
Peak Memory BW	1 GB/s	1.6 GB/s	3.2 GB/s
# of memory sockets	2	2	2
# chipset pins (mem)	~180	~200	~160
est. board layer count	4	4	4
est. board cost over PC133 sys		~\$6	~\$7 (includes 10% PCB Zo)

**RDRAM provides ~2X Bandwidth
at comparable Platform Cost to DDR**

DRAM Cost/Price

“The Hinge Factor”

- RDRAM memory cost can be competitive with alternatives
 - 4i bank RDRAM (in addition to 16D and 2x16D) planned for with next generation chipset in 2002
 - Other factors key
 - Learning curve (driven by volume)
 - License and royalty costs
- Memory Pricing eventually determined by market

More Details in DRAM Supplier Presentations

Effects of Ramping the Intel Pentium® 4 Processor

- All Pentium®4 Processors today use the Intel® 850 Chipset
 - Dual RDRAM channels
 - Aggressive system prices available today
- Targeting introduction of the SDRAM Platform in 2H '01
 - Targeted for cost sensitive segments
 - Targeted for large corporate OEMs primarily using business applications
 - Expect <1/3 of Pentium® 4 Processor volume in '01 to use SDRAM
- Next generation RDRAM chipset is planned for 2002
 - Includes 4i RDRAM memory support
 - Continuing to drive cost reduction of the RDRAM memory & platforms

The Pentium® 4 Processor Ramp will
drive a significant RDRAM ramp

Today's Pentium® 4 System Prices

COMPAQ

home and home office

\$1604



Pres
Shipp
price.

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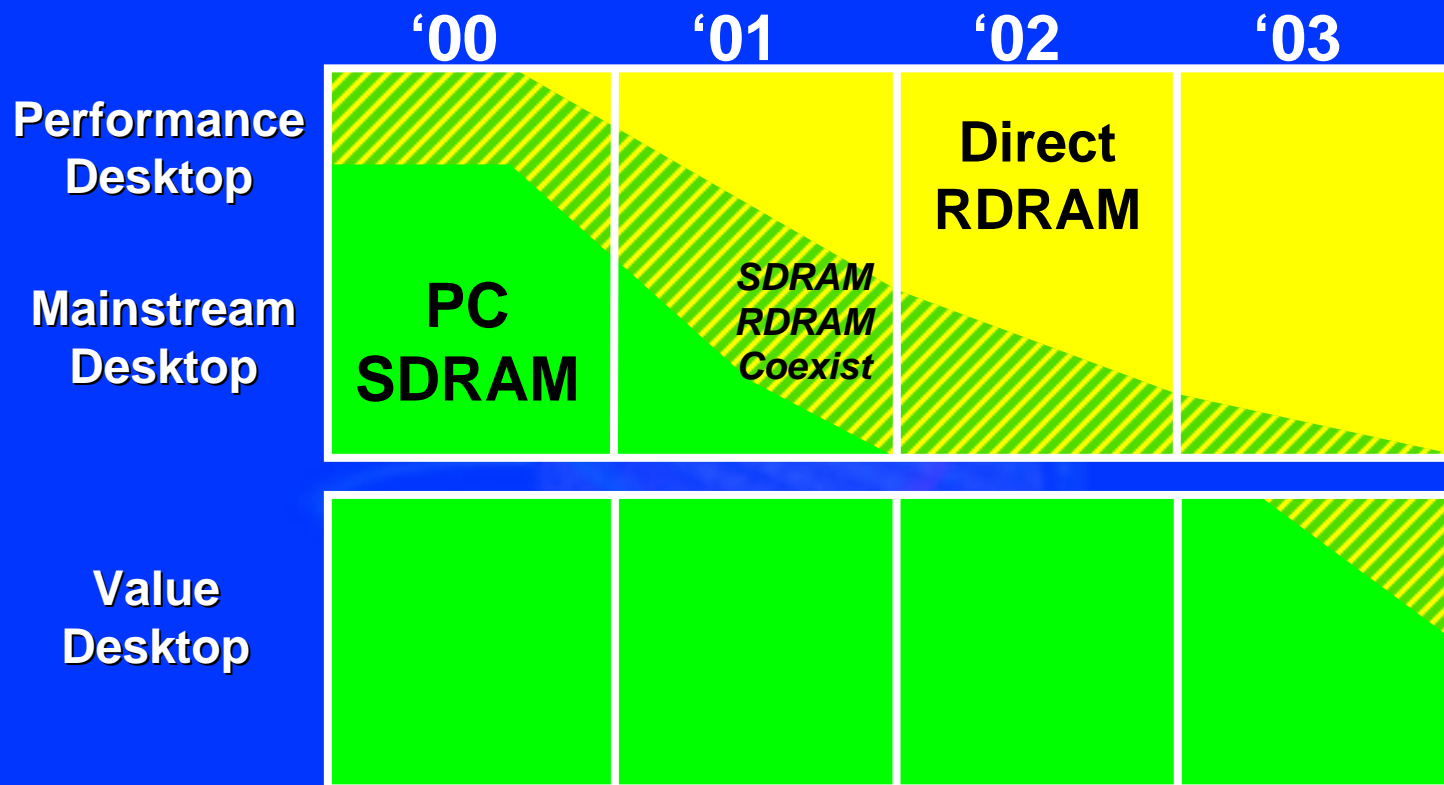
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Desktop PC Memory Roadmap



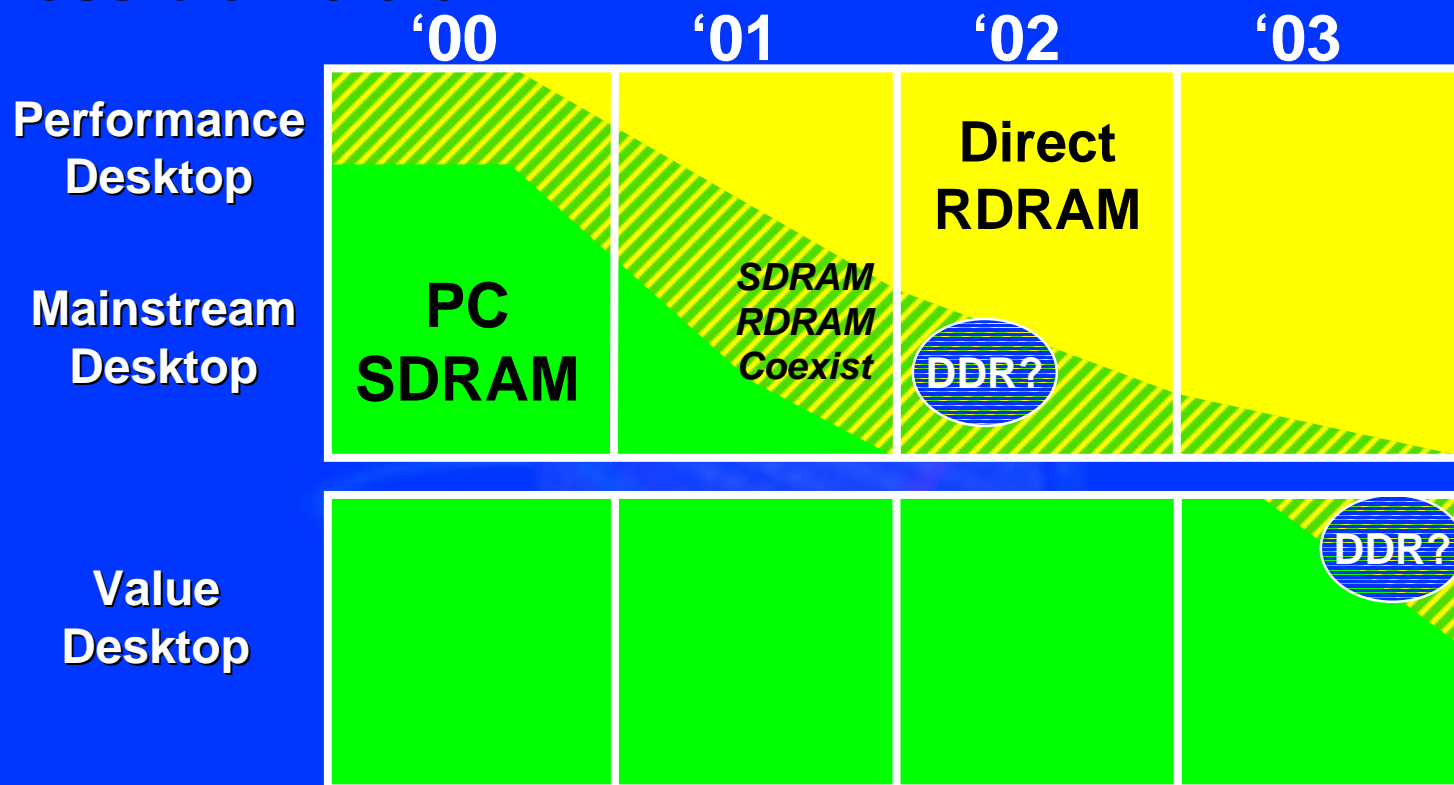
Not to Scale

- SDRAM to RDRAM transition driven by Pentium® 4 Processor ramp
- SDRAM will continue to be used in cost sensitive segments as long as it remains lowest price

All dates are target dates and subject to change.

Desktop PC Memory Roadmap

Possible Role of DDR



Not to Scale

- **DDR Solution Targeted for 1H/02**
 - Most likely role would be as SDRAM replacement
- **Competitive RDRAM pricing minimizes the role of DDR**

All dates are target dates and subject to change.

Agenda

- **Memory Strategy & Roadmap**
- **DDR Program Status**
- **RDRAM Program Status**
- **Summary**

DDR Program Status

- **Intel is Working to Deliver Robust DDR Platforms for IA CPUs**
 - Initial focus is DDR200 on Reg DIMMs for Servers
 - Also looking at:
 - Unbuffered DIMMs
 - DDR266
- **Process Includes:**
 - Documenting our issues in a Spec Addendum
 - Deploying a validation program to check for compliance
 - Developing detailed collateral for how to design with DDR and our chipsets
 - Doing extensive validation of our solutions

DDR Spec Addendum

- **Purpose of Spec Addendum is to clarify the JEDEC spec not replace it**
 - Working closely with memory suppliers to ensure they can deliver products
 - Supportive of incorporation in JEDEC spec
 - Most items are in the ballot process
- **Some of the topics covered in the DDR200 Spec Addendum**
 - Pin Assignments, initialization sequence, Electrical Characteristics and DC operating conditions, AC operating conditions, IDD Spec and conditions, AC timings for DDR 200, etc.
- **Some open issues (from desktop analysis)**
 - Output slew rate for x16 devices, RLC parameters, input clamp spec, etc.

DDR Validation Program

- **DDR200 component test capability in place**
 - Parametric and RLC tests
 - Two devices have passed, many have not
 - 3rd party test lab ready to accept DRAM samples for validation or check out
 - Contact: Advanced Validation Labs
Rhonda Duda
714-435-2630
- **System test capability expected in Q2 '01**
 - Initial testing at Intel for DDR200 on reg. DIMMs
 - Unbuffered DIMMs to follow later this year

Intel Website for Status (targeted for late Q1):
<http://developer.intel.com/technology/memory>

All dates are target dates and subject to change.

DDR Platform Collaterals and Validation

- **Expect Similar Issues to RDRAM**
 - Tight voltage margins, reference voltage stability, return path discontinuity, etc.
 - Worst case is very hard to predict
 - Important to follow design guideline (chipset specific)
- **Server Configuration Making Good Progress**
 - Details in server track
- **Desktop is Just Getting Started**
 - Extend server effort to look at unbuffered DIMMs, 4 layer PCBs, and x16 DRAMs

**Thorough Validation Will Take Time
May not be First but will be Robust**

Agenda

- Memory Strategy & Roadmap
- DDR Program Status
- **RDRAM Program Status**
- Summary

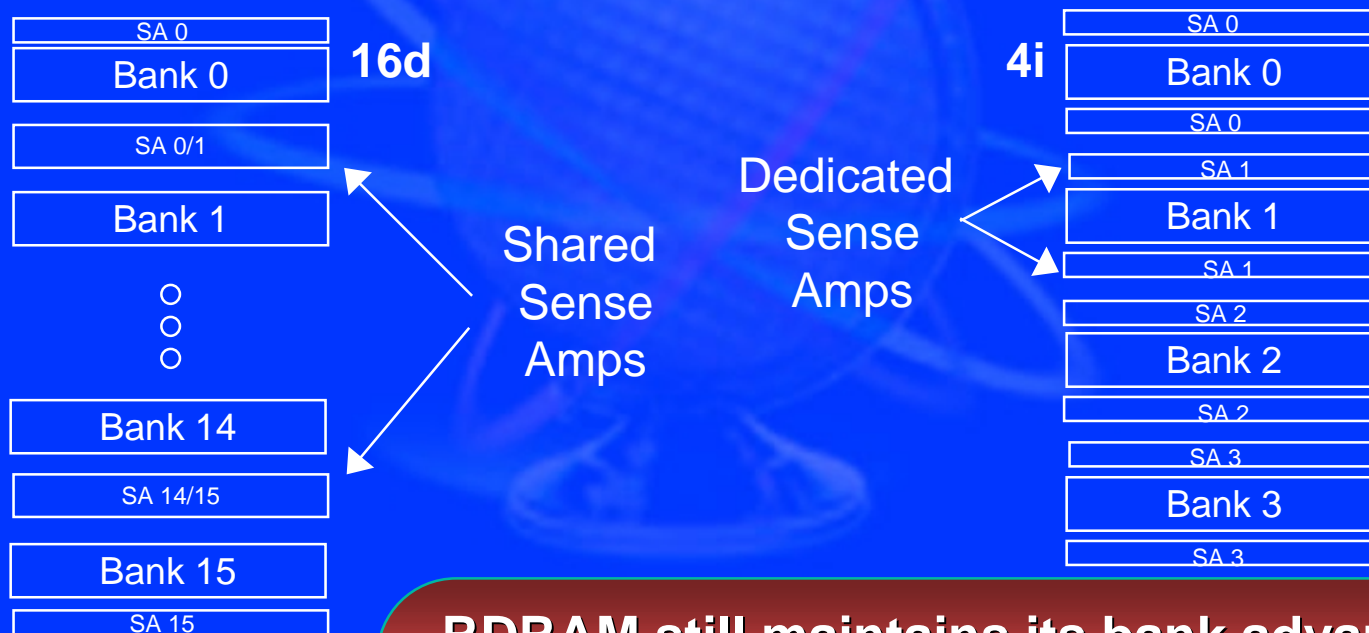
RDRAM Program Status

- **PC600/700/800 are Stable Technologies**
 - Focused on increasing bin splits, cost reduction (including 4i support), and higher density
 - Starting to Look at Higher Speed (PC1066)
- **Design Collaterals for all Chipsets**
- **Validation program in place**
 - Component (>30 devices), RIMM (>150 modules), and System (>150)
 - Clock (4 vendors), connectors (4 vendors)
 - Details at:
 - <http://developer.intel.com/technology/memory/rdram/>

More Details in DRAM Supplier Presentations

Support for 4i Architecture

- Current RDRAMs are 2x16d and 16d
 - 4i can further improve the cost structure
 - Smaller die and better redundancy coverage
- Intel currently plans to support all 3 in mid '02



**RDRAM still maintains its bank advantage
(4 devices = 16 banks)**

Agenda

- **Memory Strategy & Roadmap**
- **DDR Program Status**
- **RDRAM Program Status**
- **Summary**

Summary

- **Aggressive Pentium® 4 Processor Ramp will Drive RDRAM Ramp this Year**
- **RDRAM Provides the Best Pentium® 4 Processor Platform Now and in the Future**
- **SDRAM will be the Lowest Cost Memory**
 - Right choice for Pentium® III Processor platforms going forward
 - Good choice for low end Pentium® 4 Processor platforms
- **Server Platforms will use DDR this Year**
 - DDR200 on registered DIMMs
- **Support for DDR in the Desktop in 1H/02**
 - Extensive validation required to ensure it is robust
 - Competitive RDRAM pricing may limit role

All dates are target dates and subject to change.

ELPIDA DRAM Development

Hidemori Inukai

Vice President

Elpida Memory, Inc.

February 27, 2001



Agenda

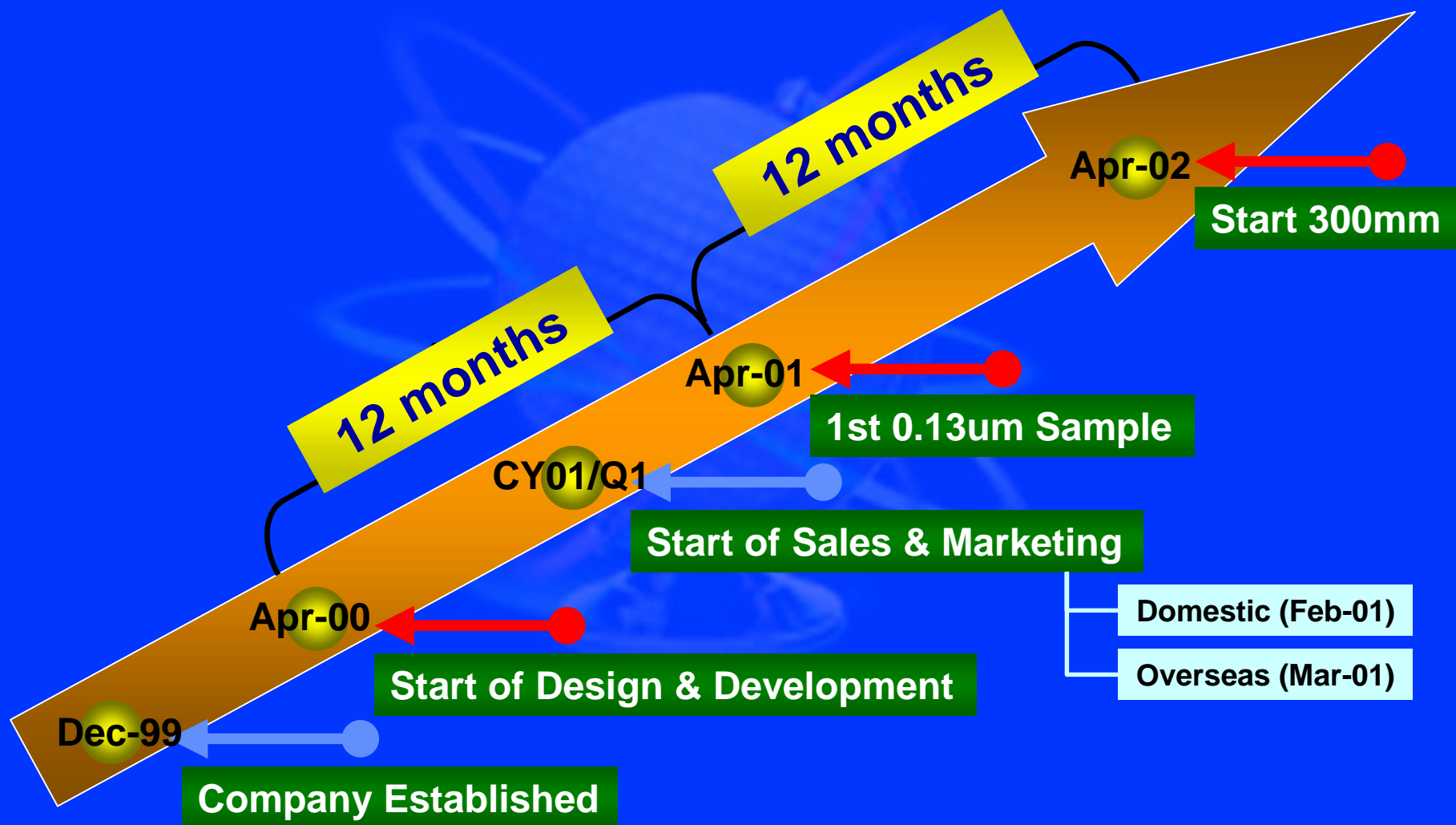
- **Company Profile**
- **DRAM Production Plan
& Development Road Map**
- **RDRAM Development Plan**
 - **Capacity expansion , Cost projection**

NEC (DRAM) + Hitachi (DRAM) = **Elpida**

- **Rich heritage from parent companies:**
 - Advanced DRAM process technology
 - Investment in R&D and capital equipment
 - Quality, reliability, dependability of products
- **New company qualities:**
 - Completely dedicated to DRAM
 - Support for all major architectures: SDR/DDR/Rambus
 - Combined resources for technology innovation and larger market presence



0.13um, 300mm Ramp, Sales Integration Major Elpida Milestones

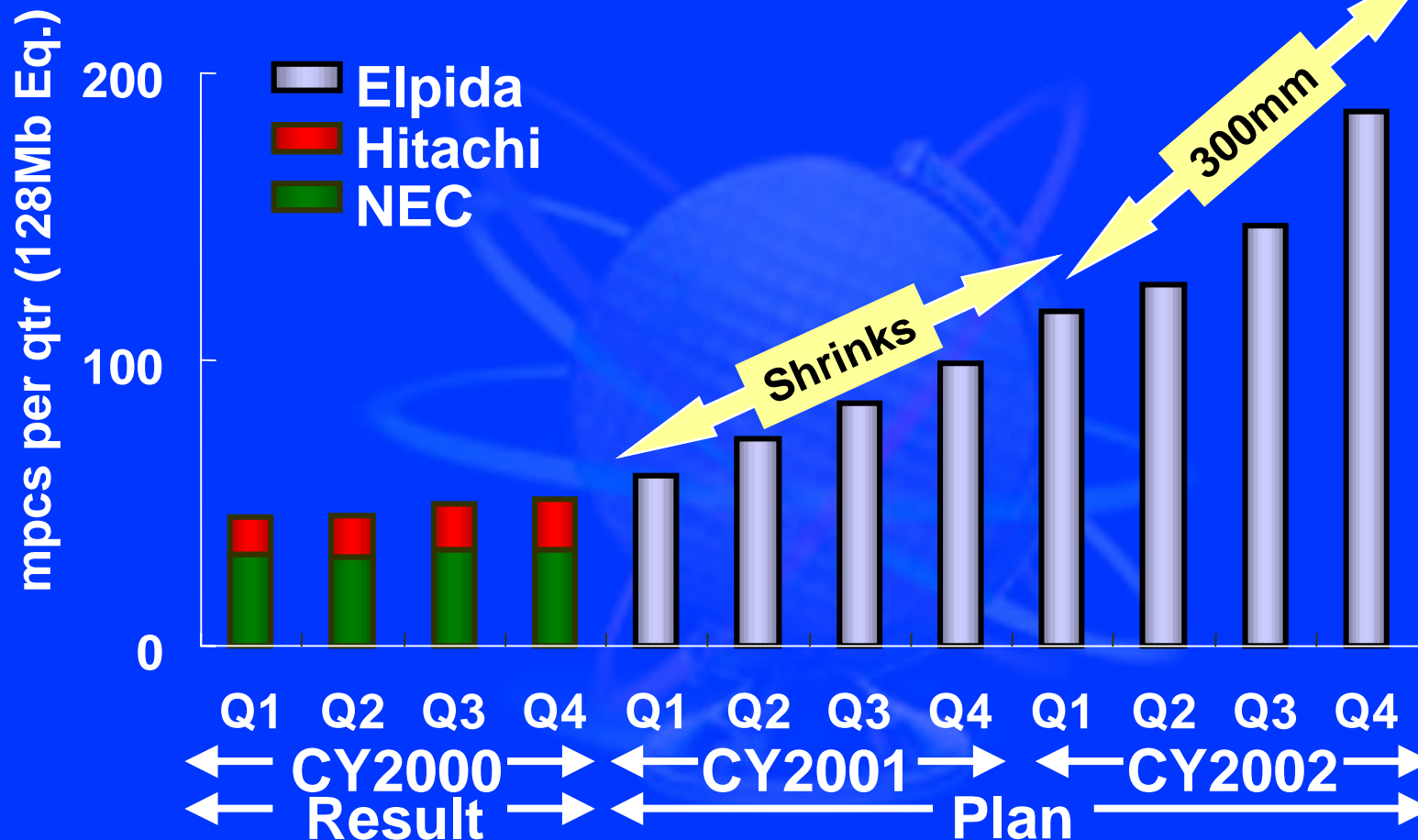


ELPIDA

Agenda

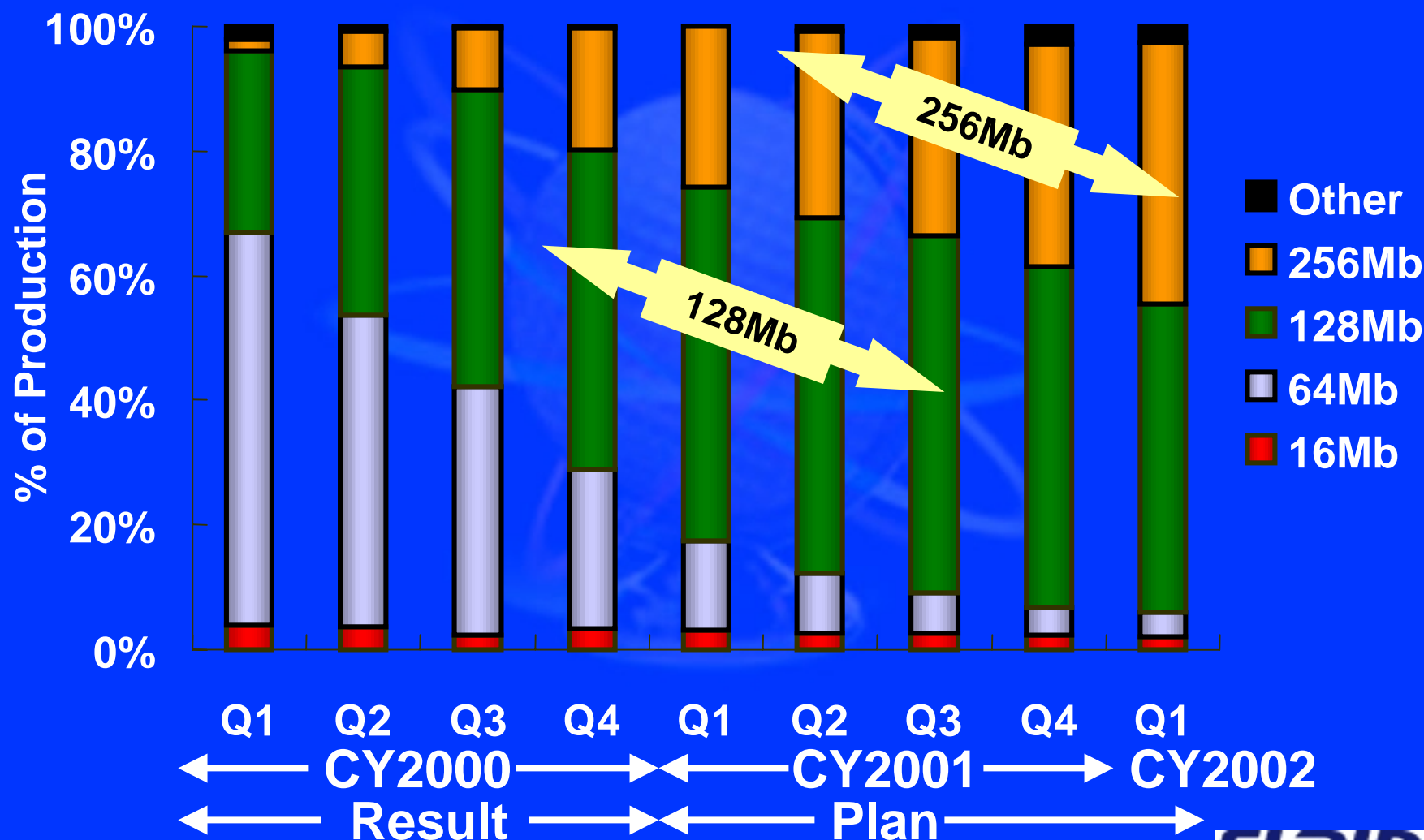
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Elpida Total Production



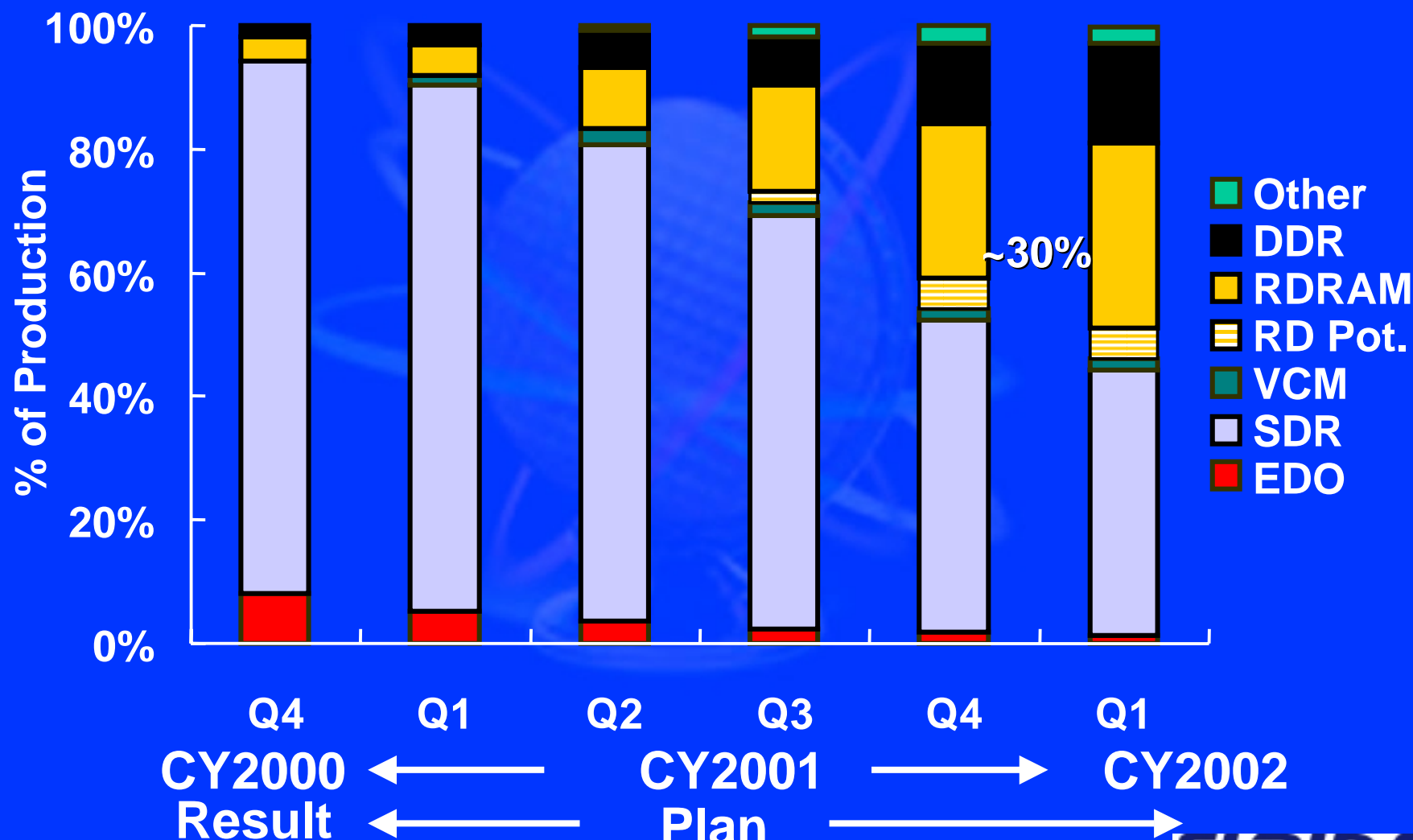
Accelerating our Growth: Shrinks & 300mm

Elpida Total Production Density Mix



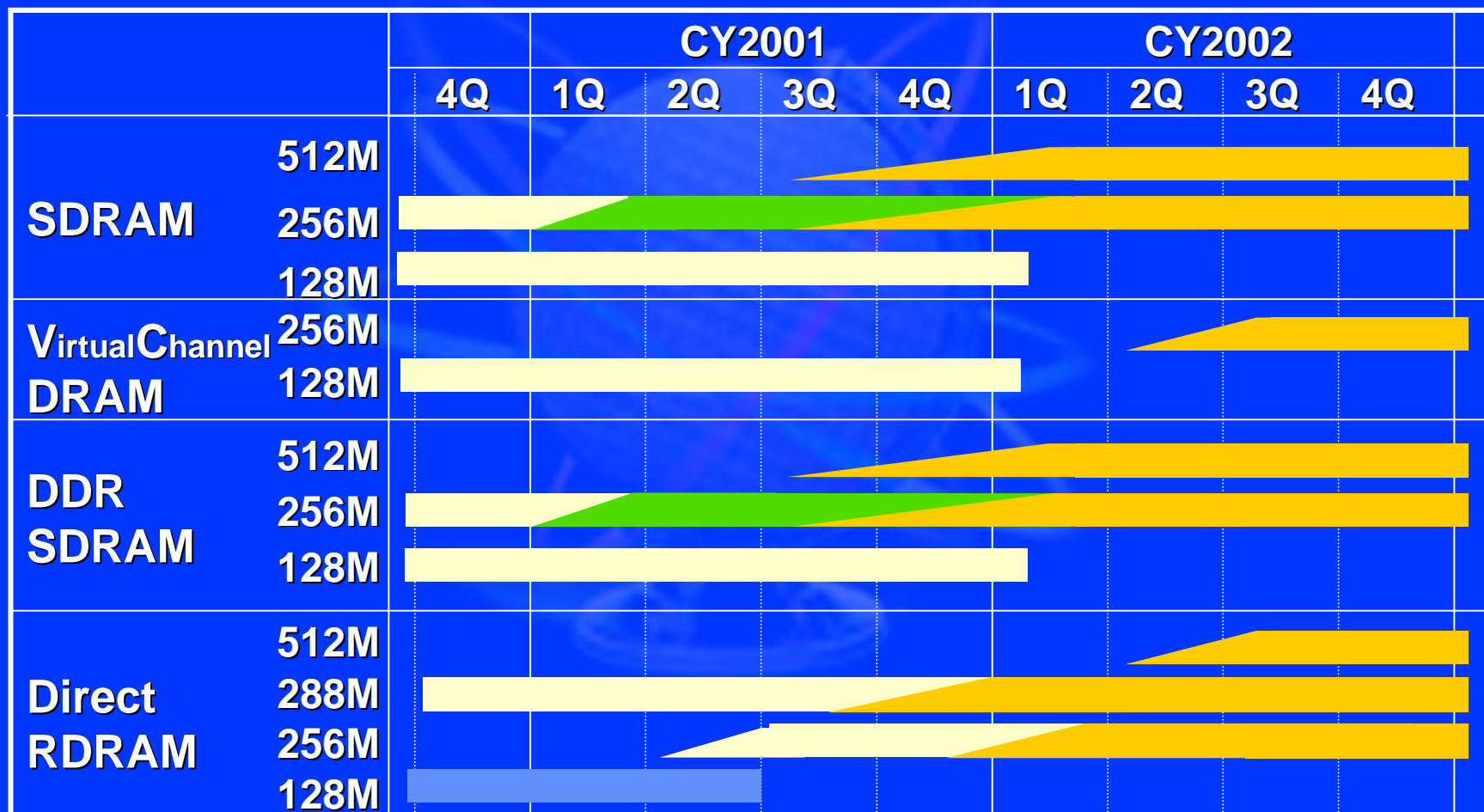
ELPIDA

Elpida Total Production Architecture Mix



Development Road Map

Full Lineup for All Major Architecture



0.22μ

0.18μ

0.15μ

0.13μ

ELPIDA

Agenda

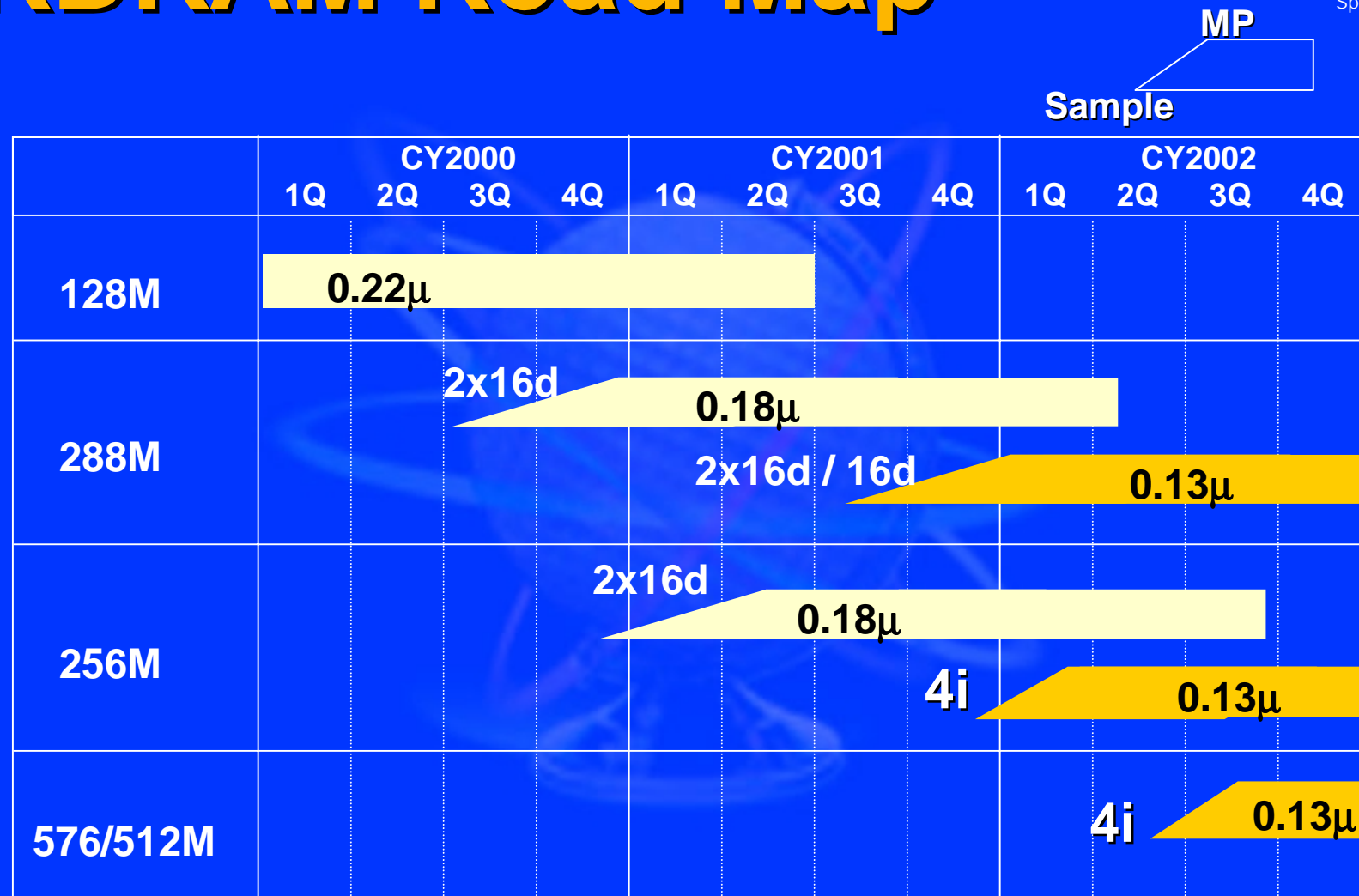
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- **RDRAM Development Plan**
 - **Capacity expansion , Cost projection**

Elpida RDRAM Development

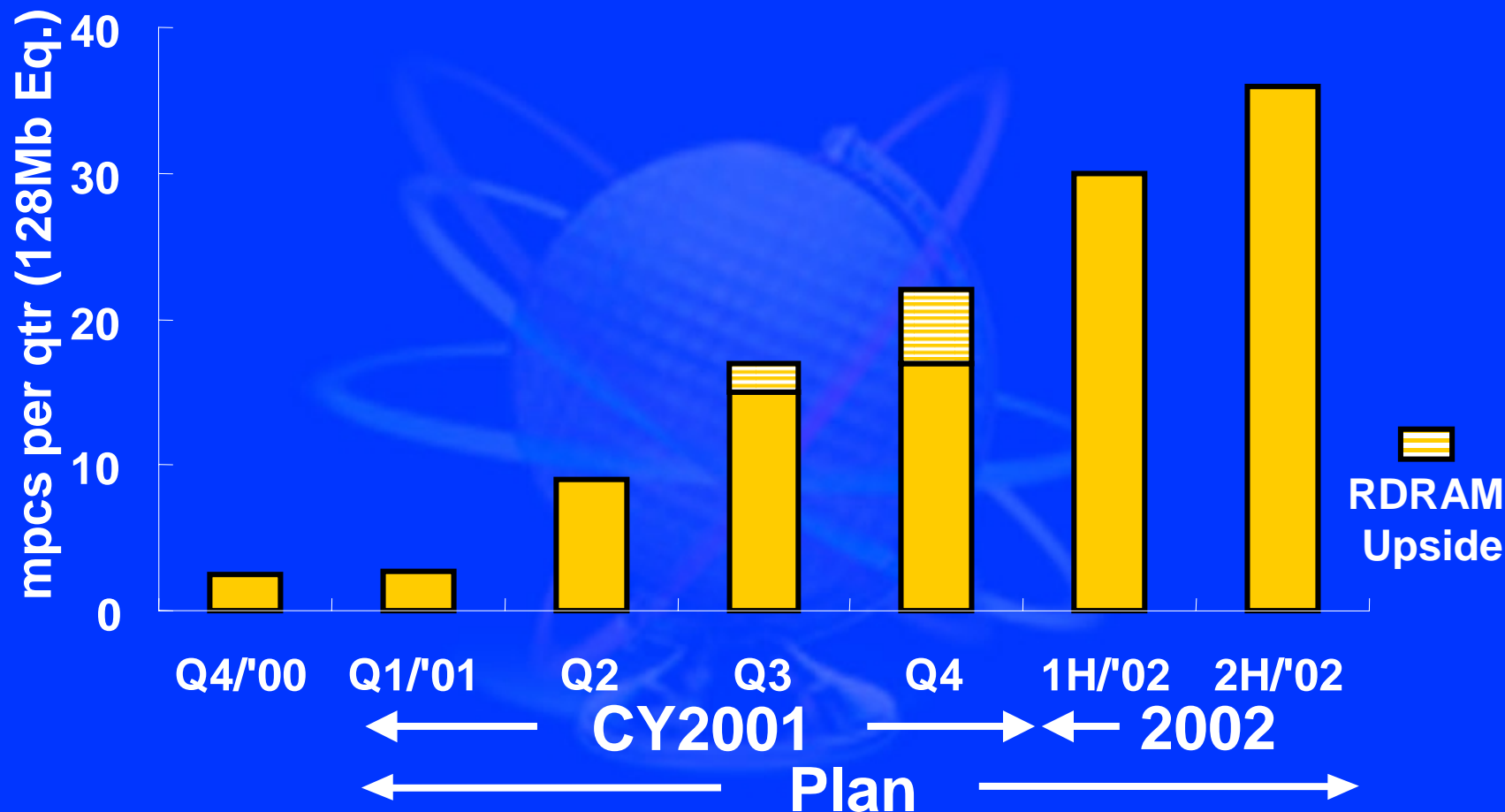
- **Most experienced and Largest RDRAM supplier since Base RDRAM**
- **First 288M RDRAM validated in worldwide**
- **Now shifting production from 128M to 288M**



RDRAM Road Map



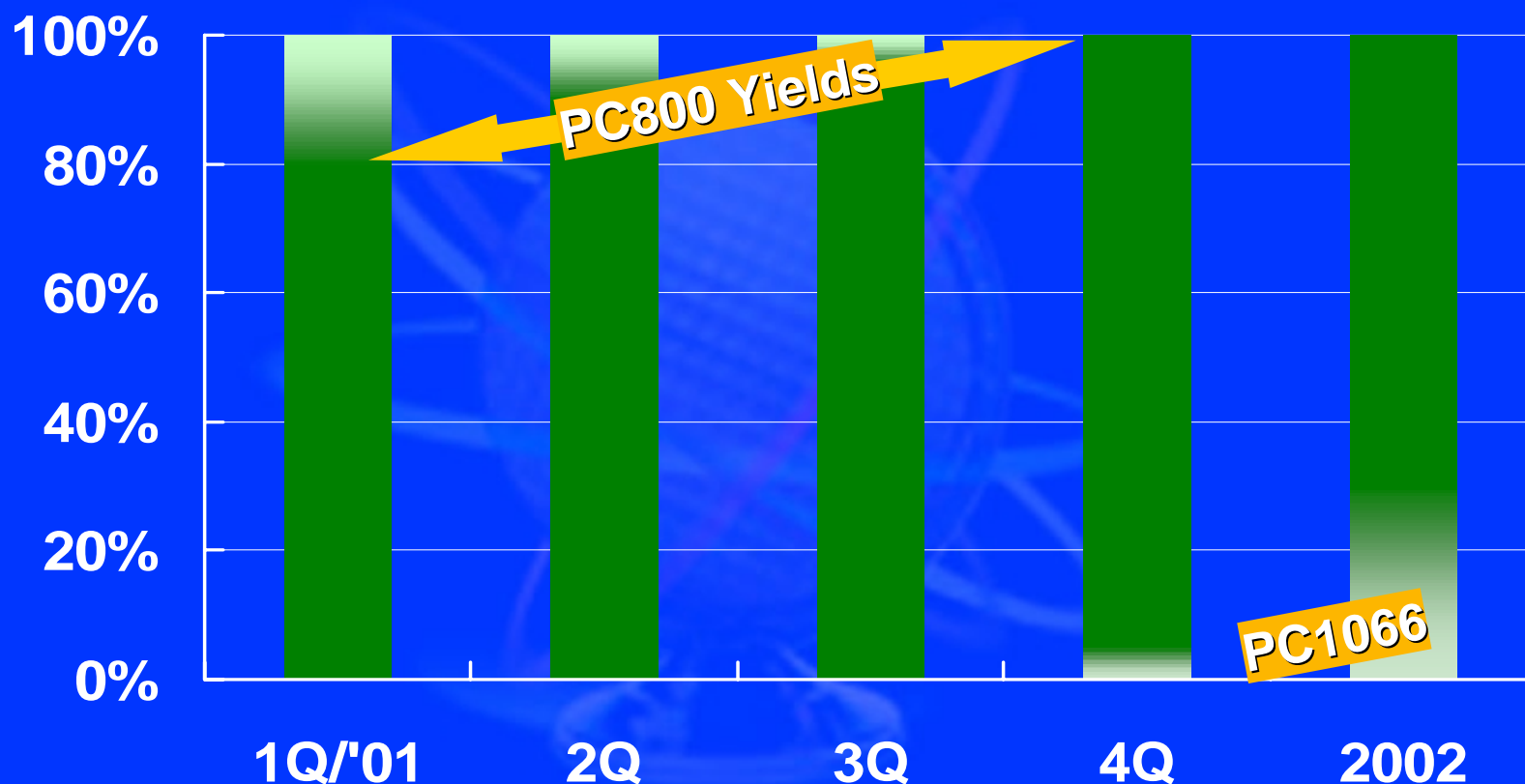
Capacity Expansion Plan



Aggressive ramp for RDRAMs



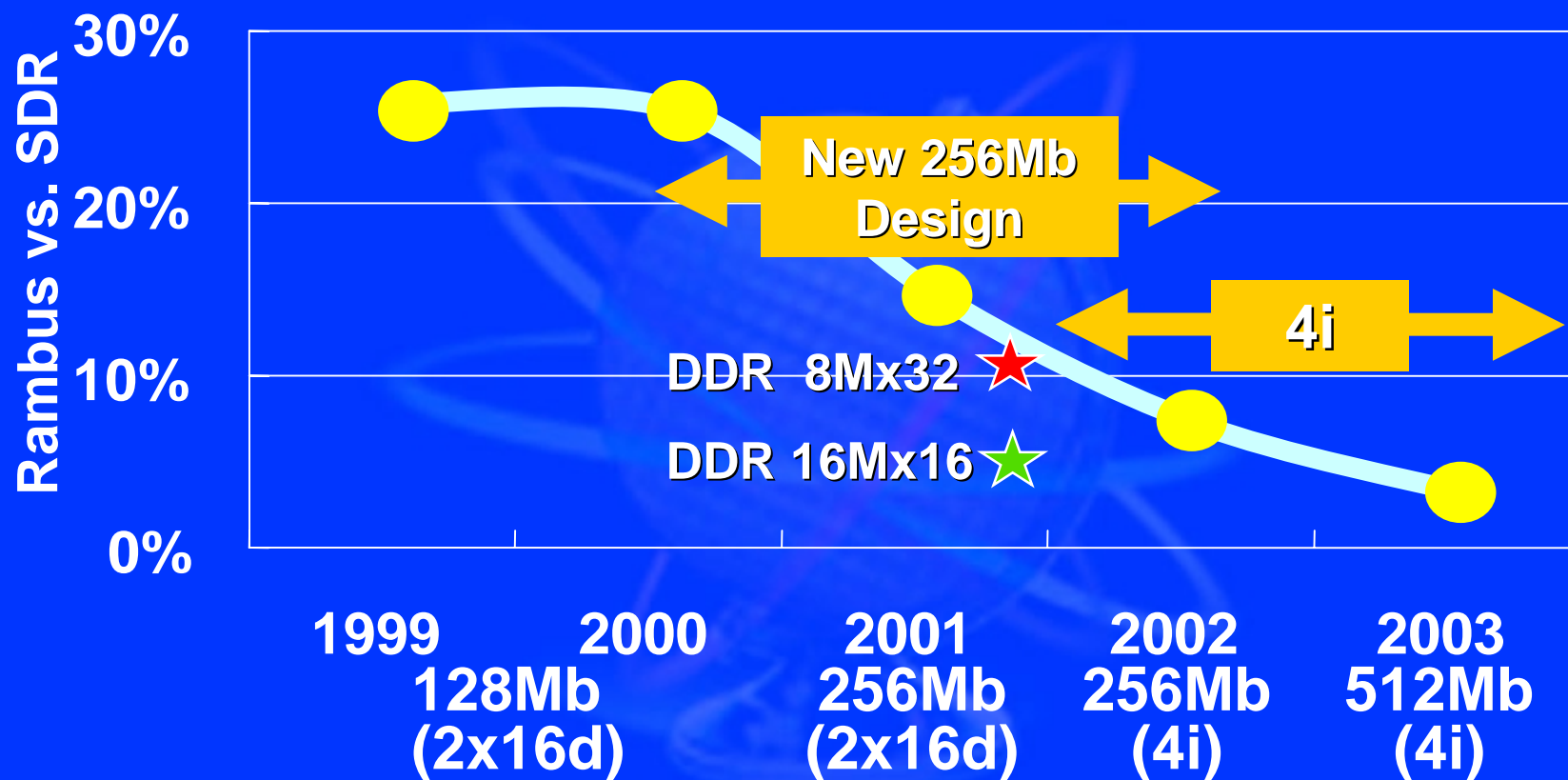
Speed Yield Transition



Accelerating our Speed Grade Improvements



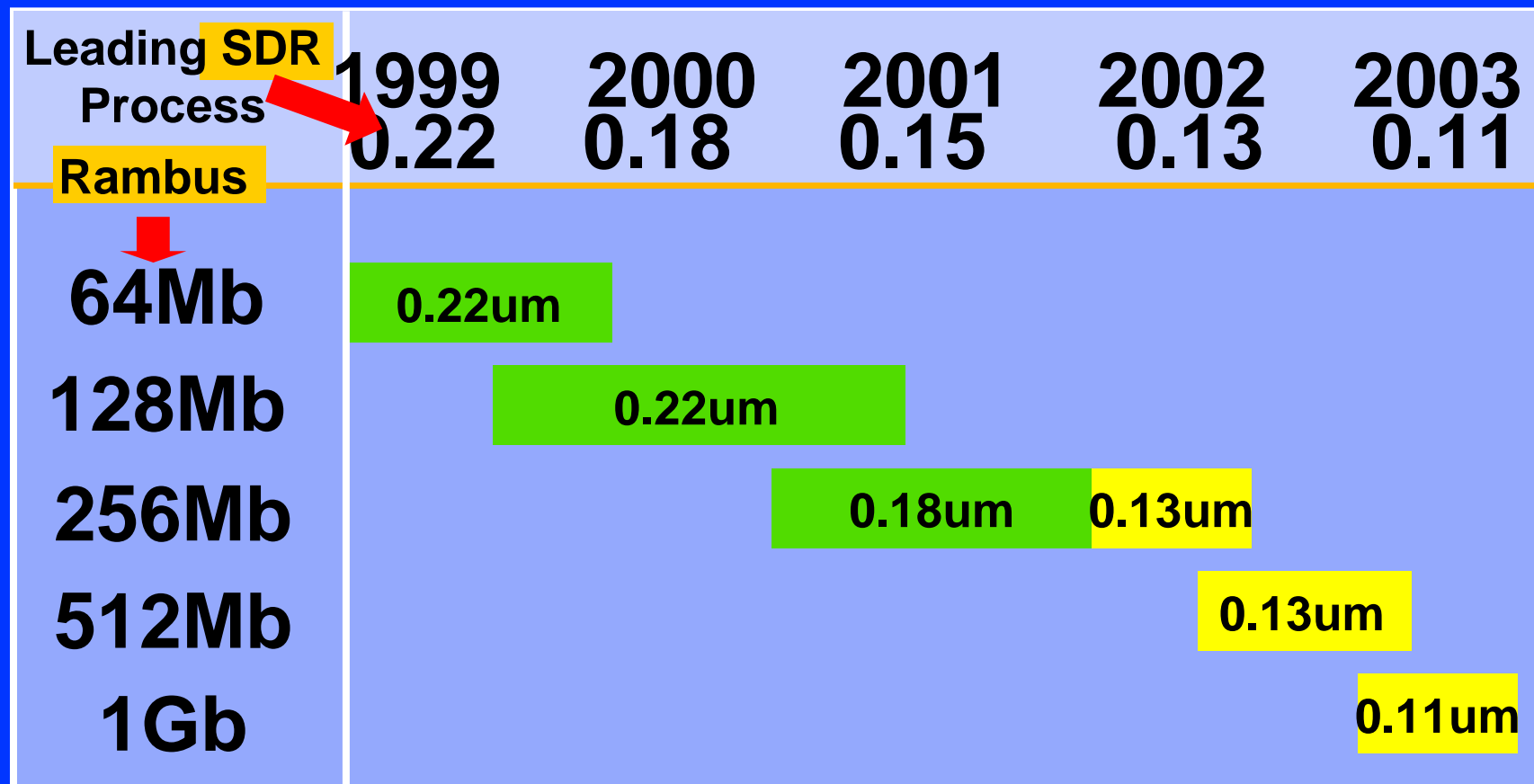
Die Overhead



Note: Densities reflect generation both ECC & non-ECC

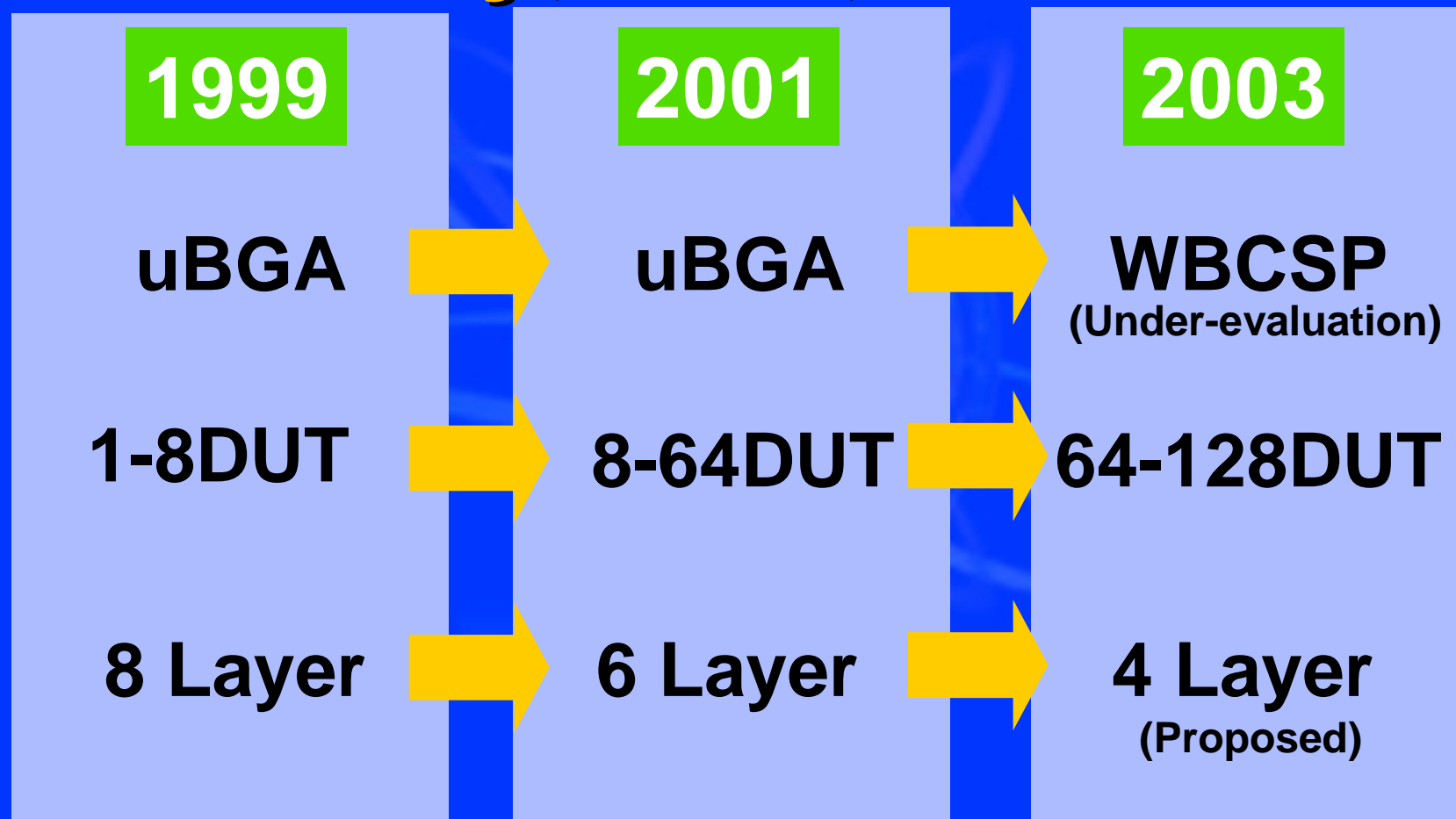
Accelerating our Design Learning Curve

Leading-Edge Process



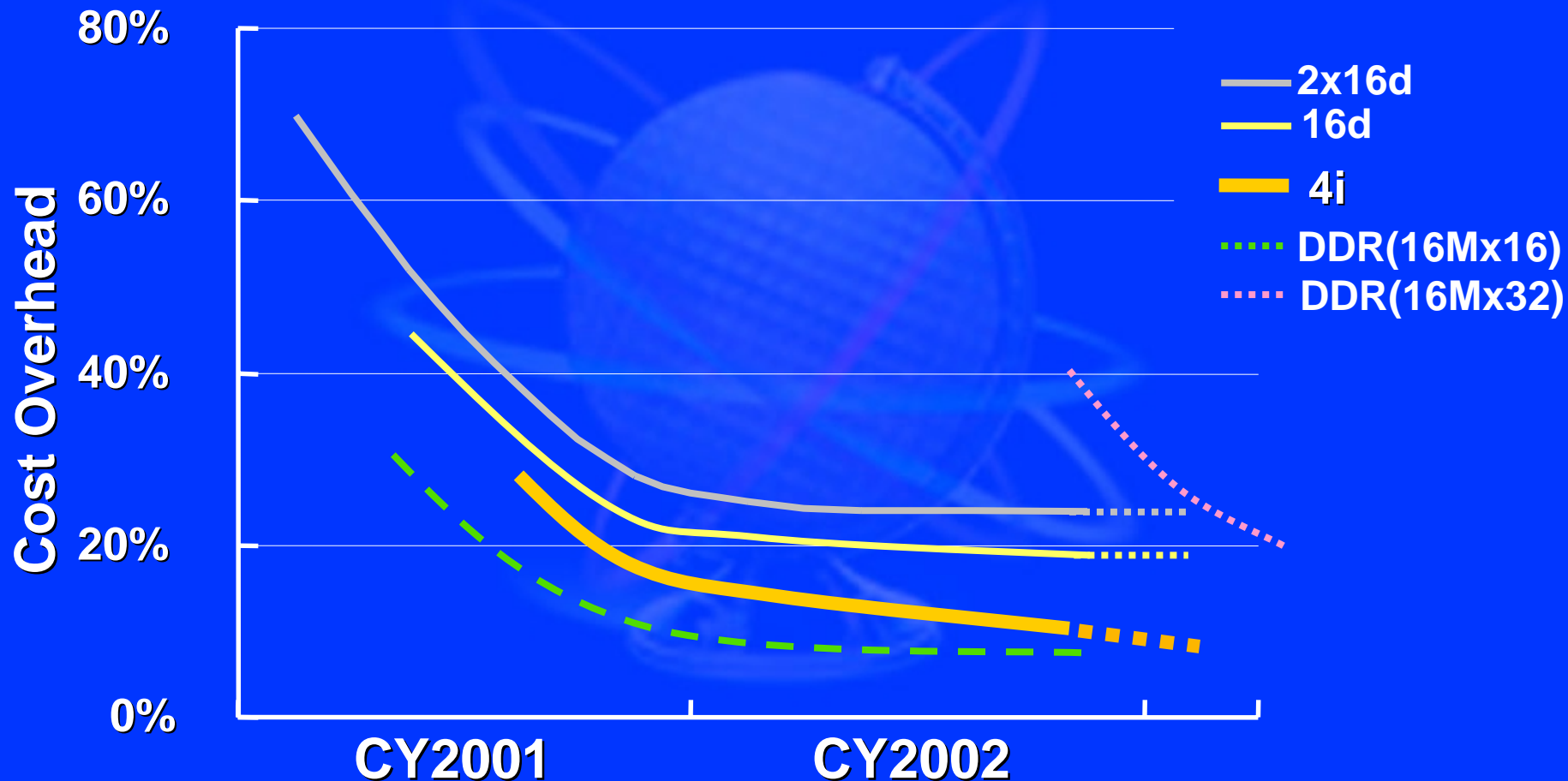
Moving Rambus to Leading Processes

Introducing Cost-effective Solutions **Assembly, Test, RIMM**



Cost Projection

128MB RIMM , 128MB DDR DIMM
vs. 128MB SDRAM DIMM



RDRAM cost projection already included royalty



CY2001-CY2003 Outlook

RDRAM Future

- Die overheads continue to shrink
- Output & Speed Yields much improved
- Back-end costs improved
- Module material costs improved
- Most Competitive Leading process

RDRAM's now more Manufacturable!
Committed to RDRAM Ramp & Promotion!
Competitive pricing for Pentium®4 Processor ramp!



Right Memory Solution for DeskTop PC

Jon Kang
Senior Vice President
Samsung Memory Division

February 27, 2001

Agenda

- **Company Profile**
- **Samsung DRAM Update**
- **Ready for Pentium®4 Processor Ramp**
- **Conclusion**

Kiheung Plant

Since 1983

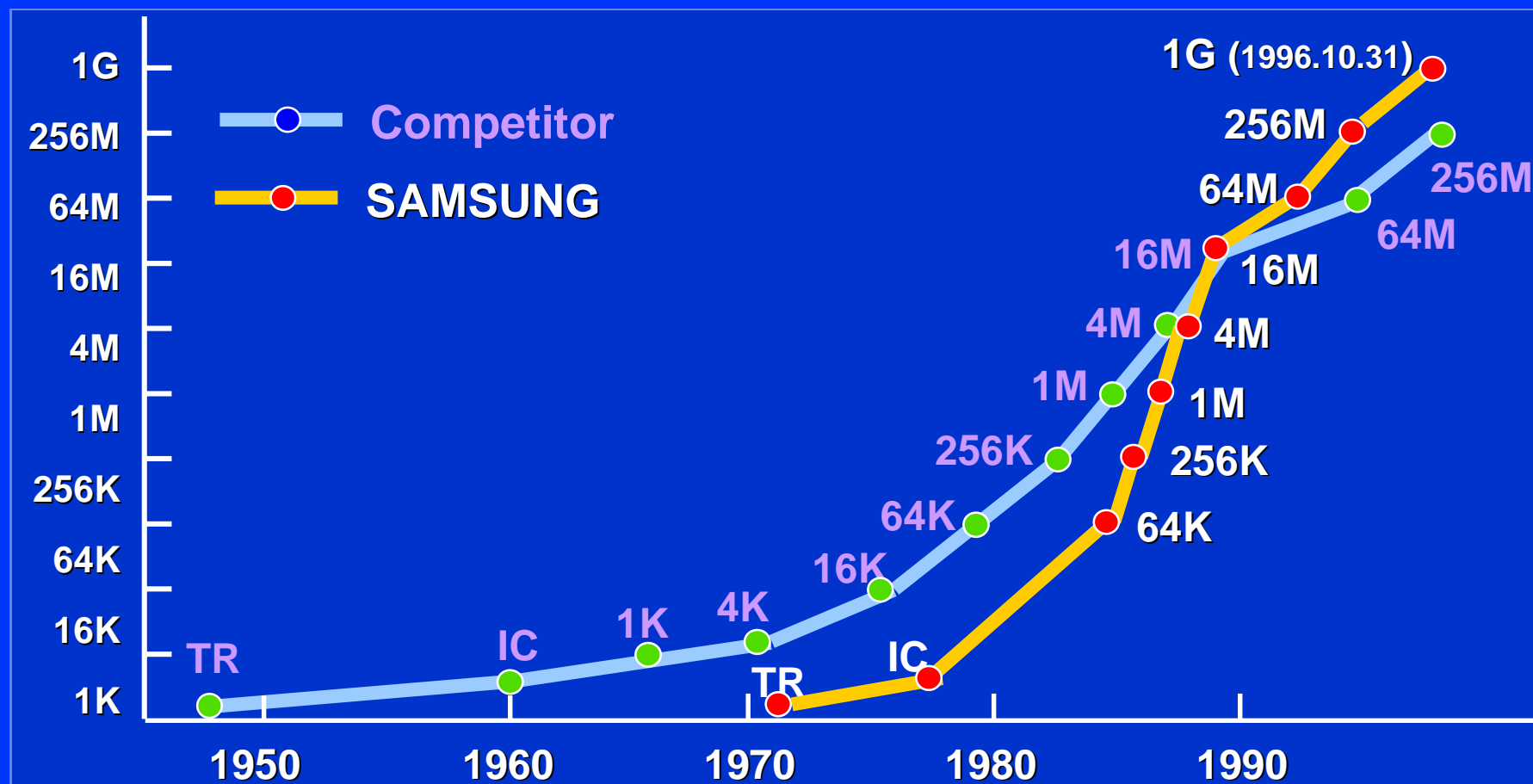


Samsung Memory History

'74	Started Semiconductor Business
'83	Developed 64K DRAM
'92	Ranked as No.1 DRAM Supplier
'94	Developed 256M DRAM
'95	Ranked as No.1 SRAM Supplier
'96	Developed 1G DRAM
'97	Developed DDR SDRAM
'99	Developed 1G NAND Flash Memory
'99	Start Mass Production of 256M DRAM & Rambus DRAM
'00	Developed 512M SDRAM(DDR SDRAM)

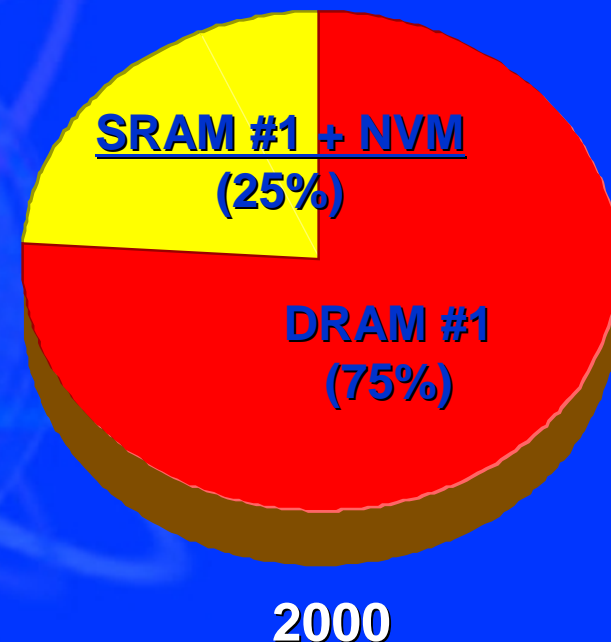
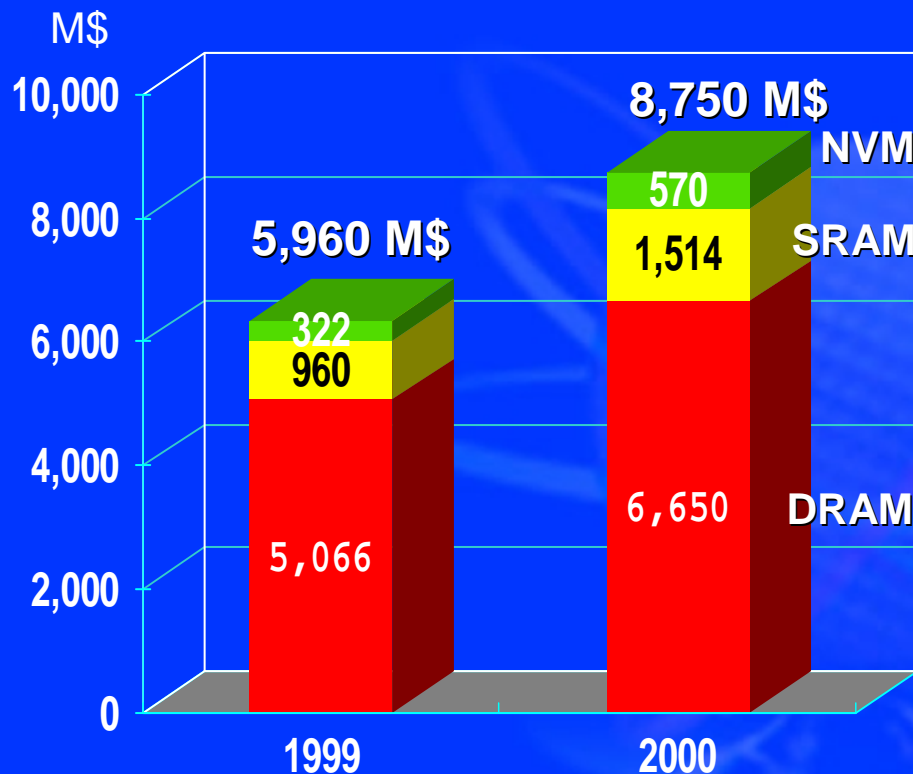
The Leader in Memory Technology

DRAM Technology Development



DRAM Technology Leader !

Samsung Memory Revenue



Samsung has been the largest Memory Supplier since 1993

Agenda

- Company Profile
- **Samsung DRAM Update**
- Ready for Pentium®4 Processor Ramp
- Conclusion

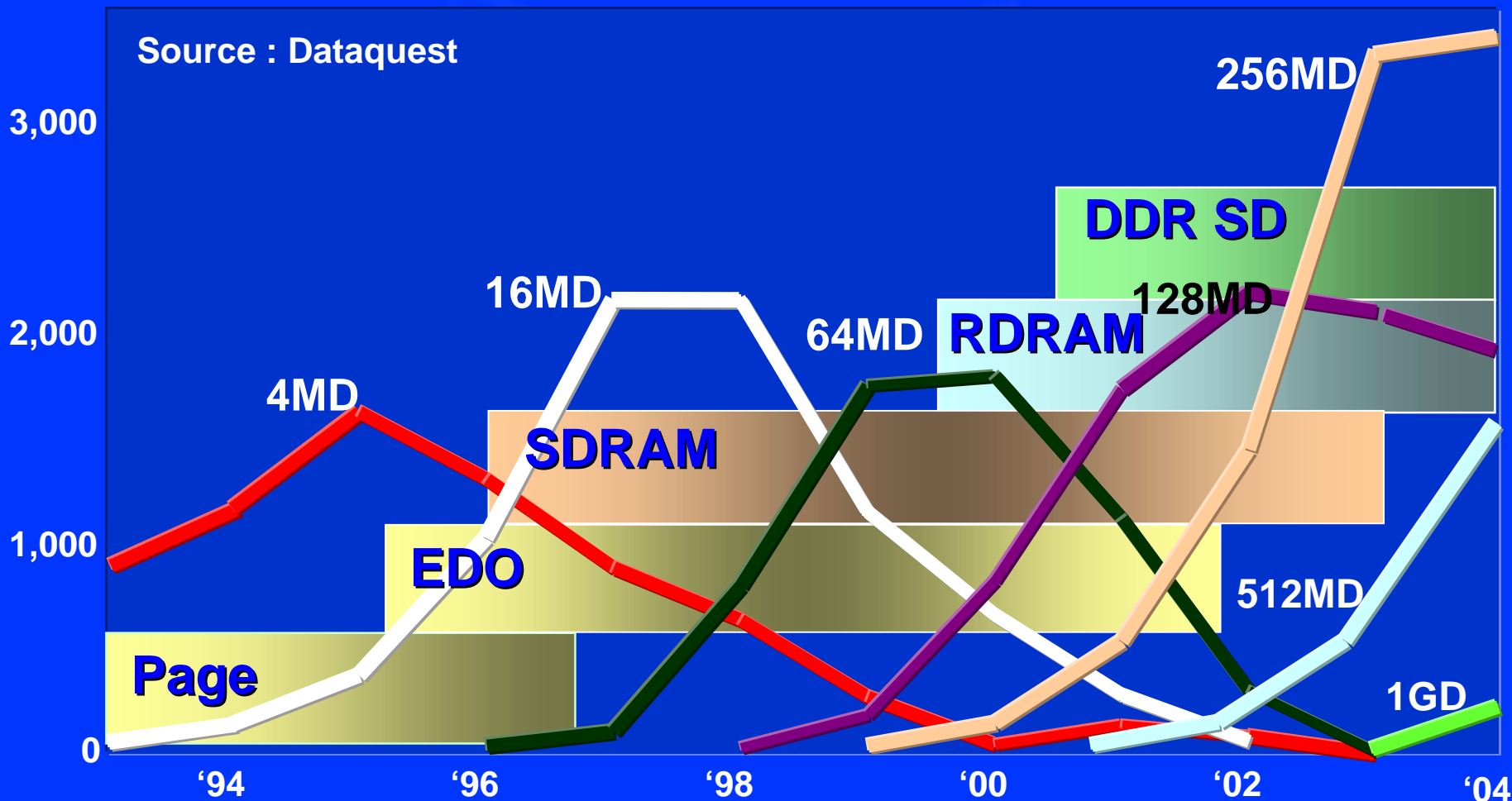
Paradigm Shift for Memory

- **High Density only**
 - 1Mb -> 4Mb -> 16Mb -> 64Mb -> 128Mb
-> 256Mb -> 512Mb
- **Multiple DRAM Architecture**
 - EDO, Sync PC100/PC133, DDR 200/266,
RDRAM
- **Right Memory depends on Application**

DRAM Production Shift Trend based on Market Demand

(WW, Mpcs)

Source : Dataquest



Samsung RDRAM status

- Improving cost structure

- Higher Yields : **Approaching SDRAM**
- Volume Production : **60Mpcs(64Mb eq.) in 2000,**
> 240Mpcs in 2001
- Flexible Architecture : **2x16d, 16d, 4i**
- Higher Density means less Overhead : **128Mb -> 256Mb**

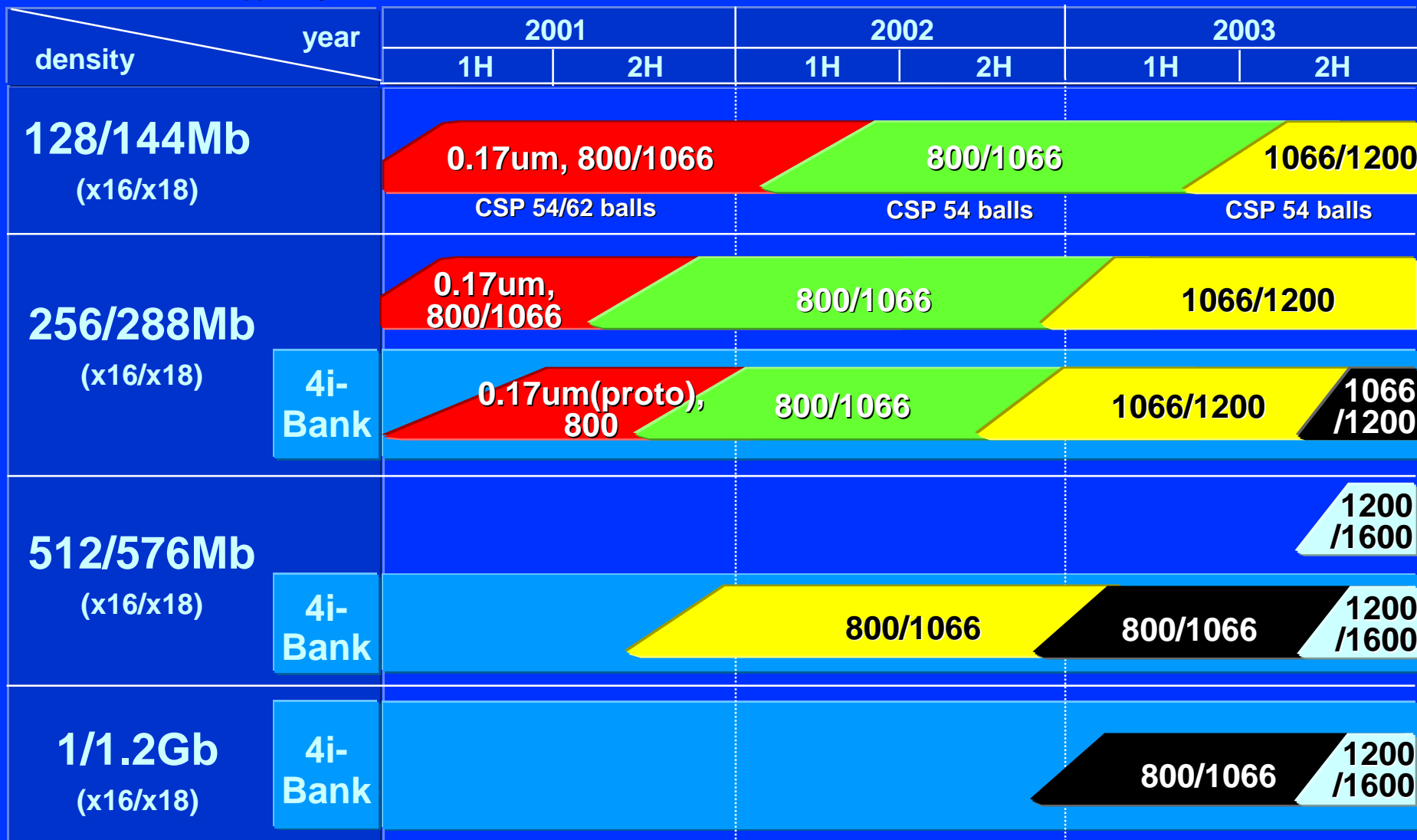
- High Yield to PC800

Faster, Denser, Volume at lower cost now !!

RDRAM Roadmap

Speed(Mbps)

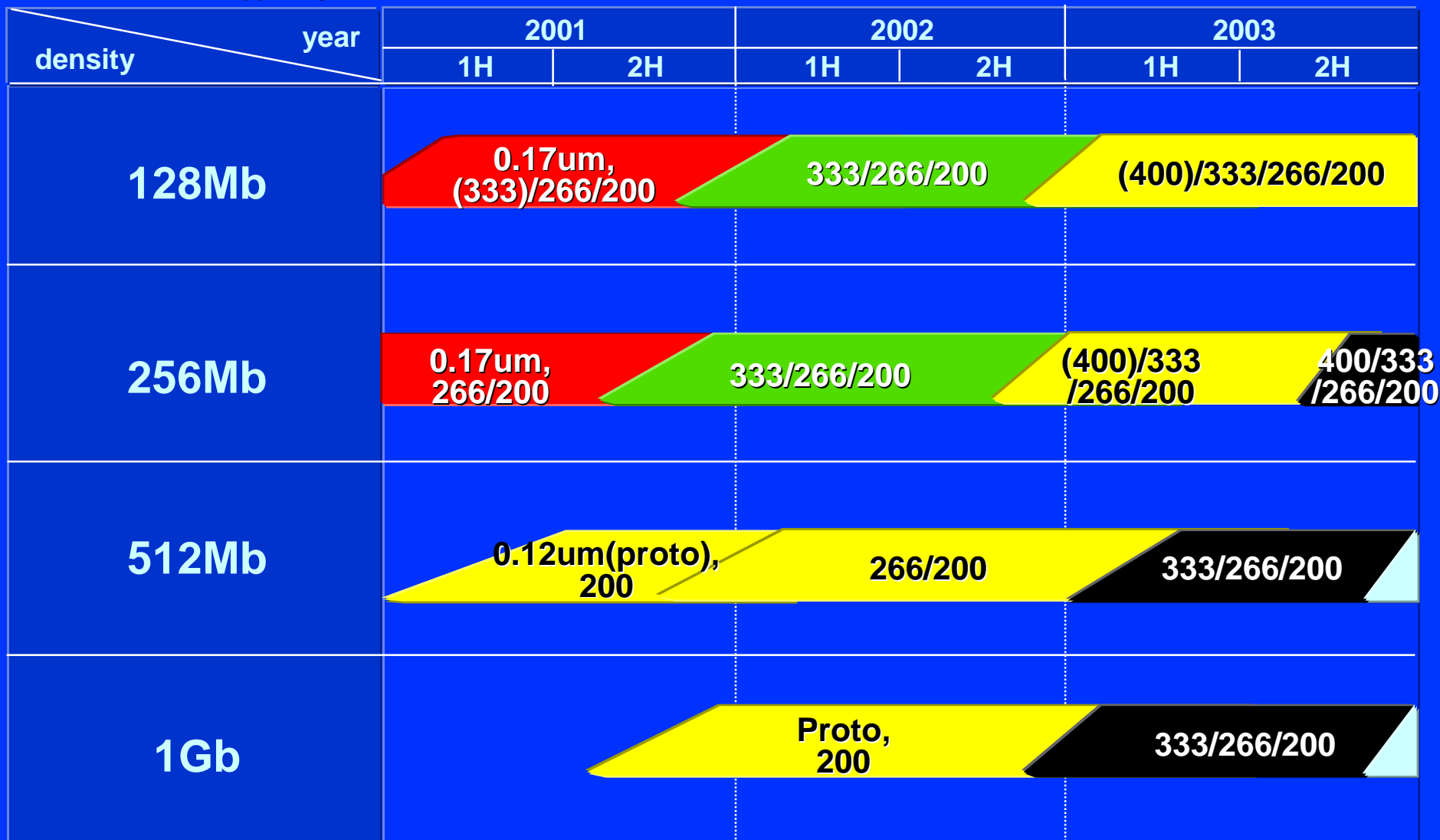
E/S M/P Vcc = 2.5V



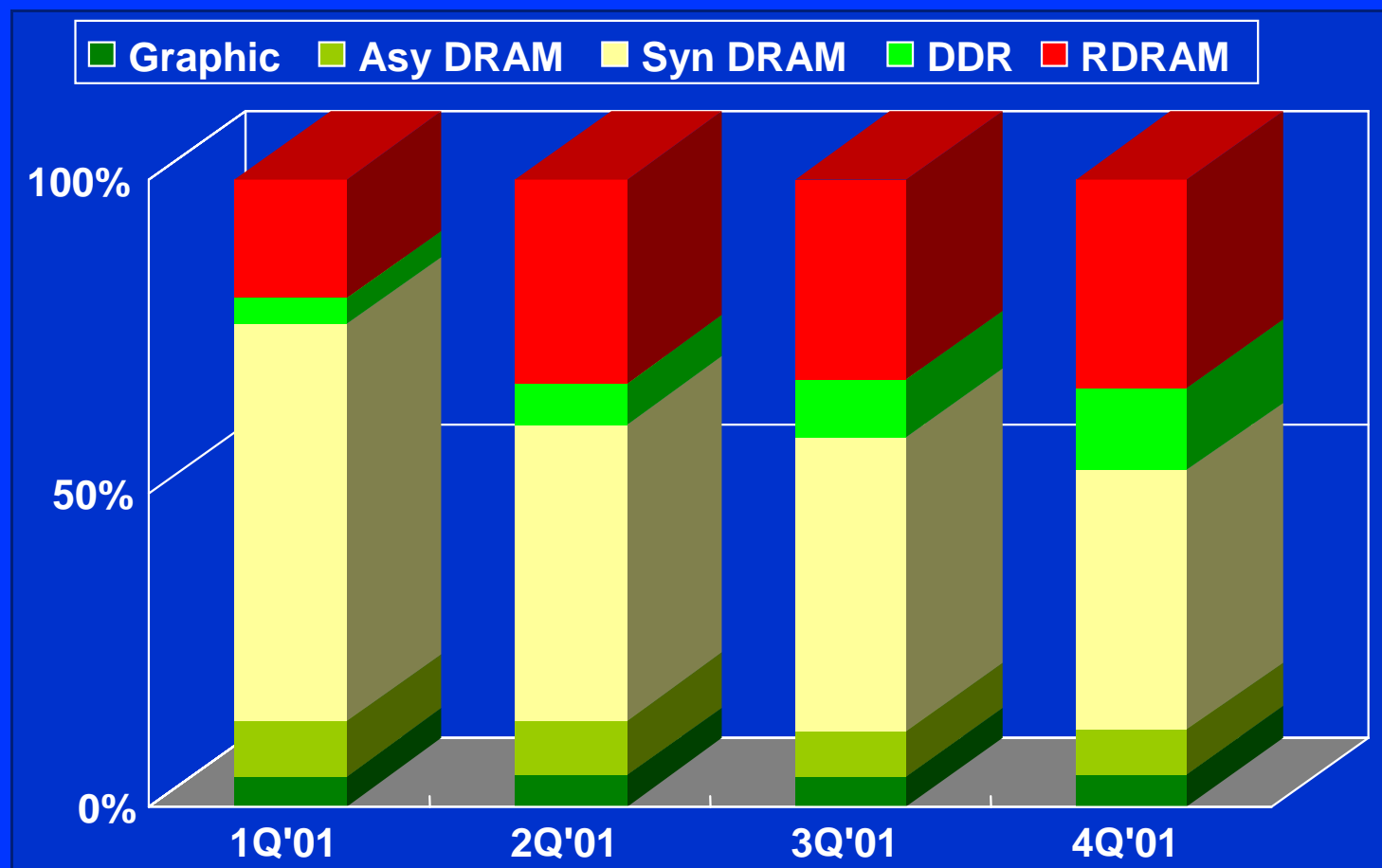
DDR SDRAM Roadmap

Speed(Mbps)

E/S M/P Vcc = 2.5V



DRAM Production Mix Plan

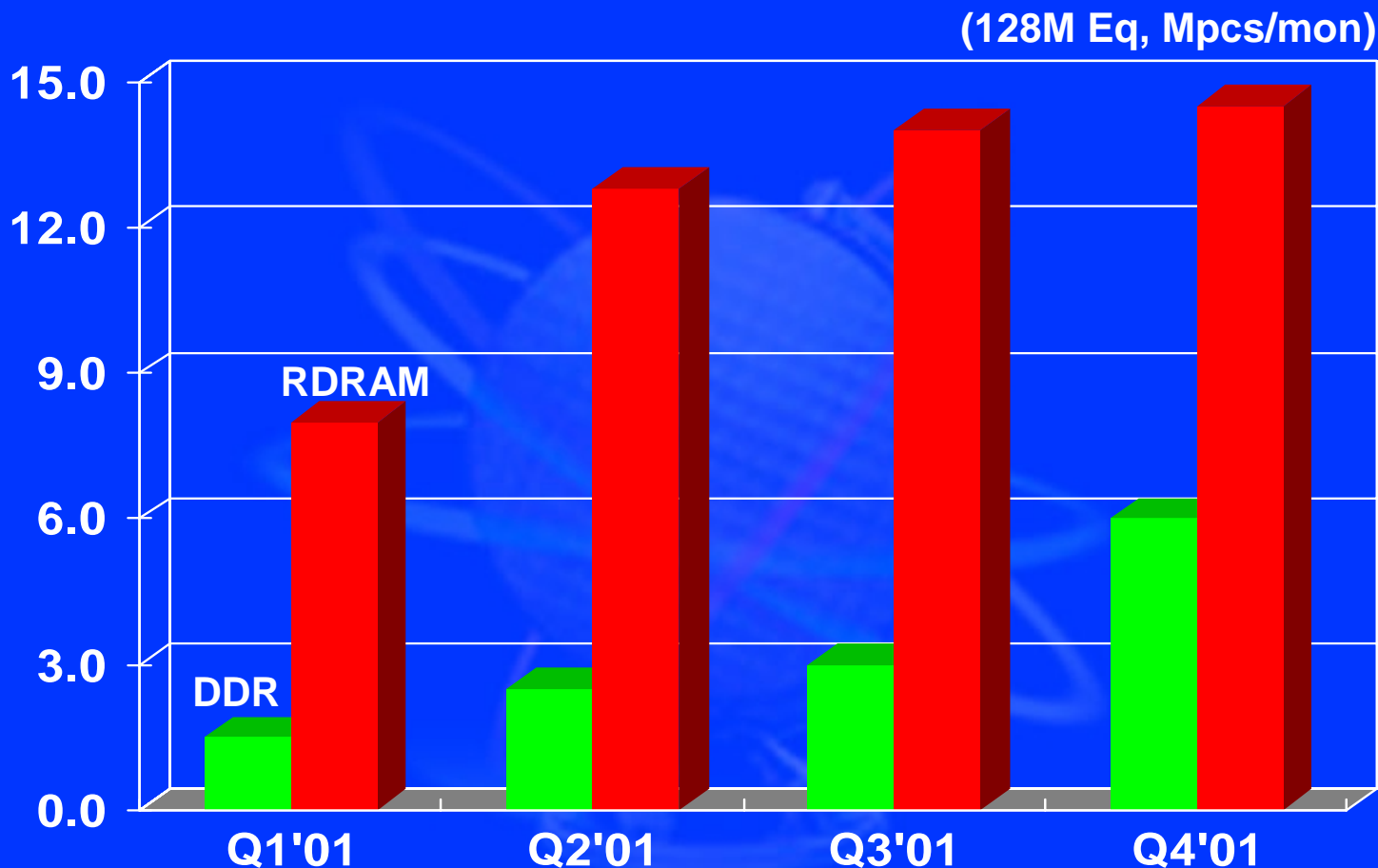


Volume Ramp-up of Advanced Products

Agenda

- Company Profile
- Samsung DRAM Update
- **Ready for Pentium®4 Processor Ramp**
- Conclusion

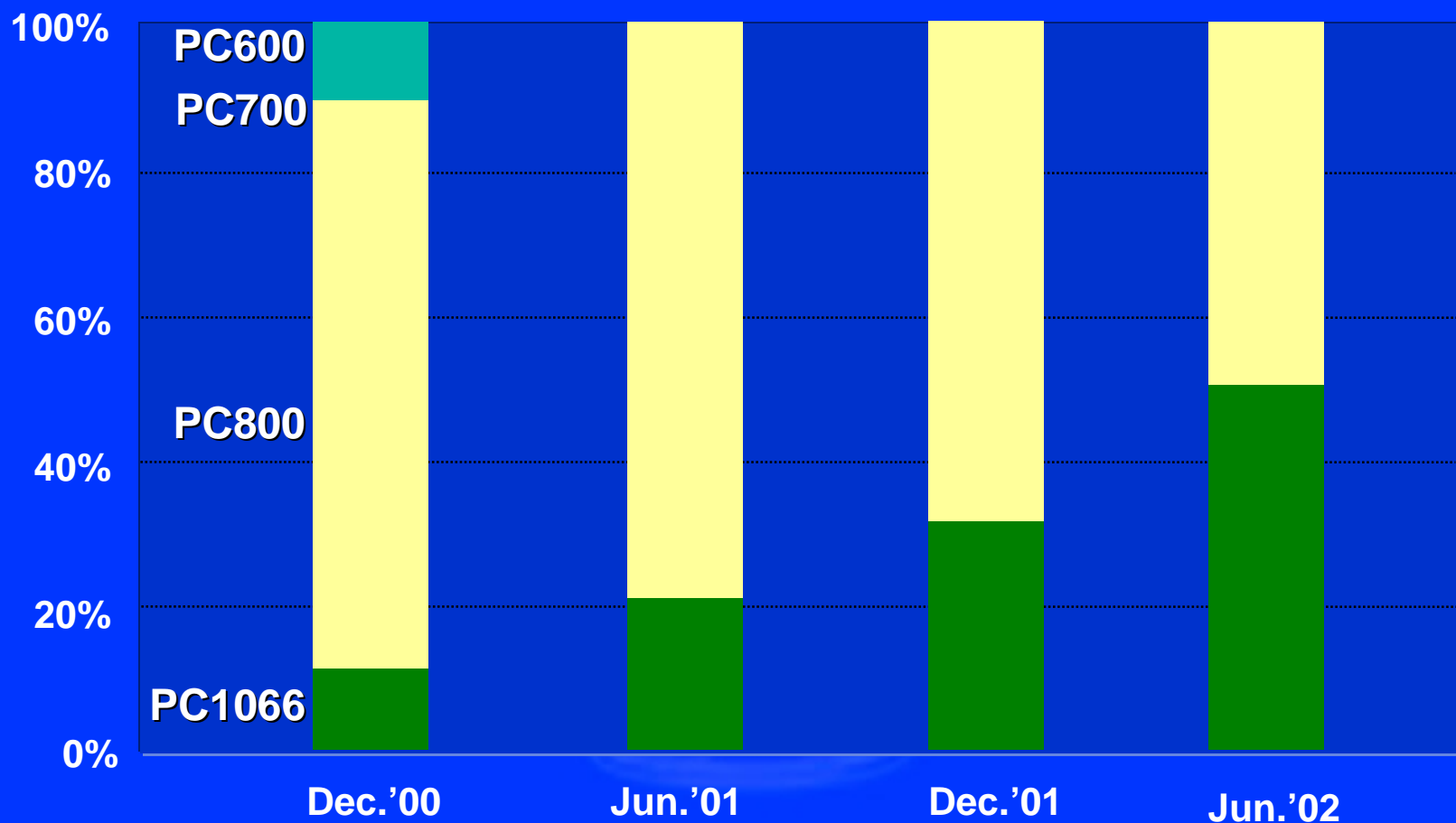
2001 RDRAM & DDR Production Plan



* Production Volume will be increased by Market demand

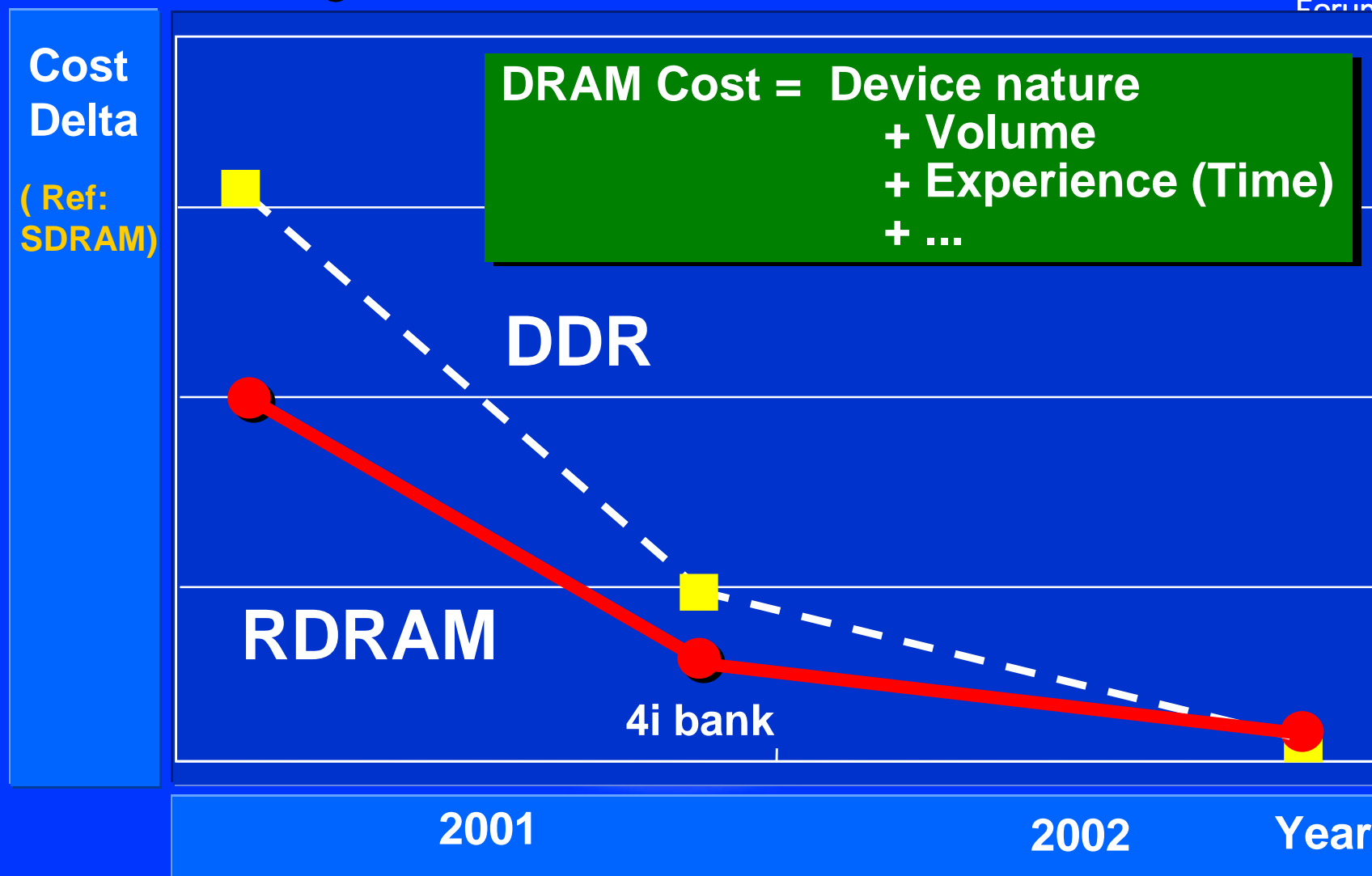
Rapidly Increasing RDRAM Volume

RDRAM Speed Portion Forecast



100% Yield to PC800

Cost Projection (Module Base)



Expect 5% cost to DDR

SDRAM Cost Reduction Milestone

	1H'01	2H'01	1H'02	2H'02
Density (Die Penalty)	128Mbit (~15%)	256Mbit (~10%)	256Mbit (~5%)	512Mbit (~1%)
Bank	2x16d	2x16d/16d	4i	4i
PKG	uBGA	uBGA	WBCSP	Low cost CSP
RIMM	8 Layer	6 Layer	6 Layer	4/6 Layer
Others	<ul style="list-style-type: none"> Yield & Test time are being improved and almost same as SDRAM from '01 end. 			

- More availability, better cost structure.

Agenda

- **Company Profile**
- **Samsung DRAM Update**
- **Ready for Pentium®4 Processor Ramp**
- **Conclusion**

Samsung DRAM Solution for Intel Platform

- **RDRAM is the best cost/performance solution for Pentium® 4 systems.**
 - RDRAM is proven technology and in high volume production
 - Cost structure is in place to achieve a competitive price to support Pentium® 4 ramp
- **DDR SDRAM is targeting Server application.**
 - Enough performance to support wide bus architecture in Server
 - Will take time -> volume usage -> to approach price parity to SDRAM

Samsung is locked & loaded to support Pentium® 4 ramp with plentiful RDRAM

Toshiba DRAM Strategy

Shozo Saito

General Manager

DRAM Dept. Memory Division

Toshiba Semiconductor Company

February 27, 2001

Agenda

- **Introduction of Toshiba Semiconductor**
- **Current RDRAM product status**
- **RDRAM roadmap**
- **DDR status**
- **Production Capacity**
- **Cost Reduction Program**
- **Summary**

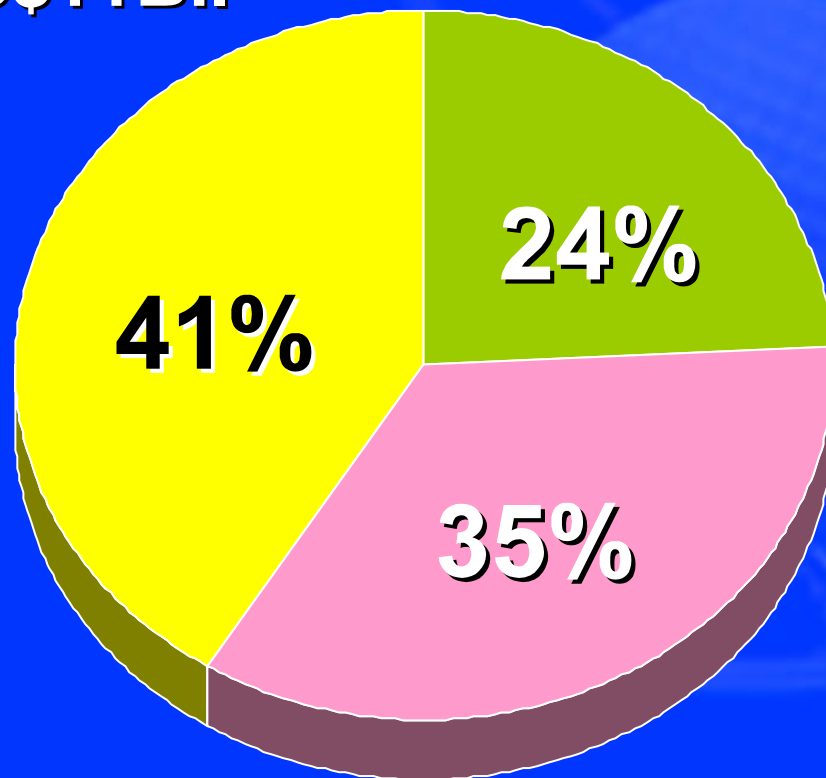
WW Semiconductor Ranking

RANKING	1996	1997	1998	1999	2000
1	INTEL	INTEL	INTEL	INTEL	INTEL
2	NEC	NEC	NEC	NEC	TOSHIBA
3	MOTOROLA	MOTOROLA	MOTOROLA	TOSHIBA	NEC
4	HITACHI	TI	TOSHIBA	SAMSUNG	SAMSUNG
5	TOSHIBA	TOSHIBA	TI	TI	TI
6	TI	HITACHI	SAMSUNG	MOTOROLA	MOTOROLA
7	SAMSUNG	SAMSUNG	HITACHI	HITACHI	STM
8	FUJITSU	FUJITSU	PHILIPS	ST MICRO	HITACHI

Source: Gartner/Dataquest

Toshiba Semiconductor Sales Forecast

US\$11Bil



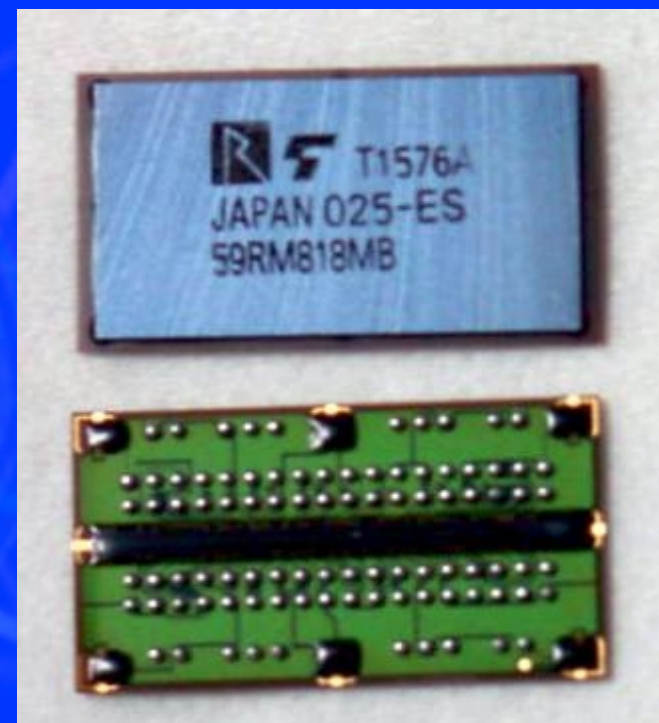
FY2000

Current RDRAM product status

- **Components:**
 - 128Mb / 144Mb : Mass Production
 - 288Mb / 256Mb : Ramp Up
- **Modules:**
 - 64MB to 512MB
 - ◆ Non-ECC
 - ◆ ECC
 - Under development:
 - ◆ 2 devices RIMM (64MB)
 - ◆ 32 devices RIMM (1GB)

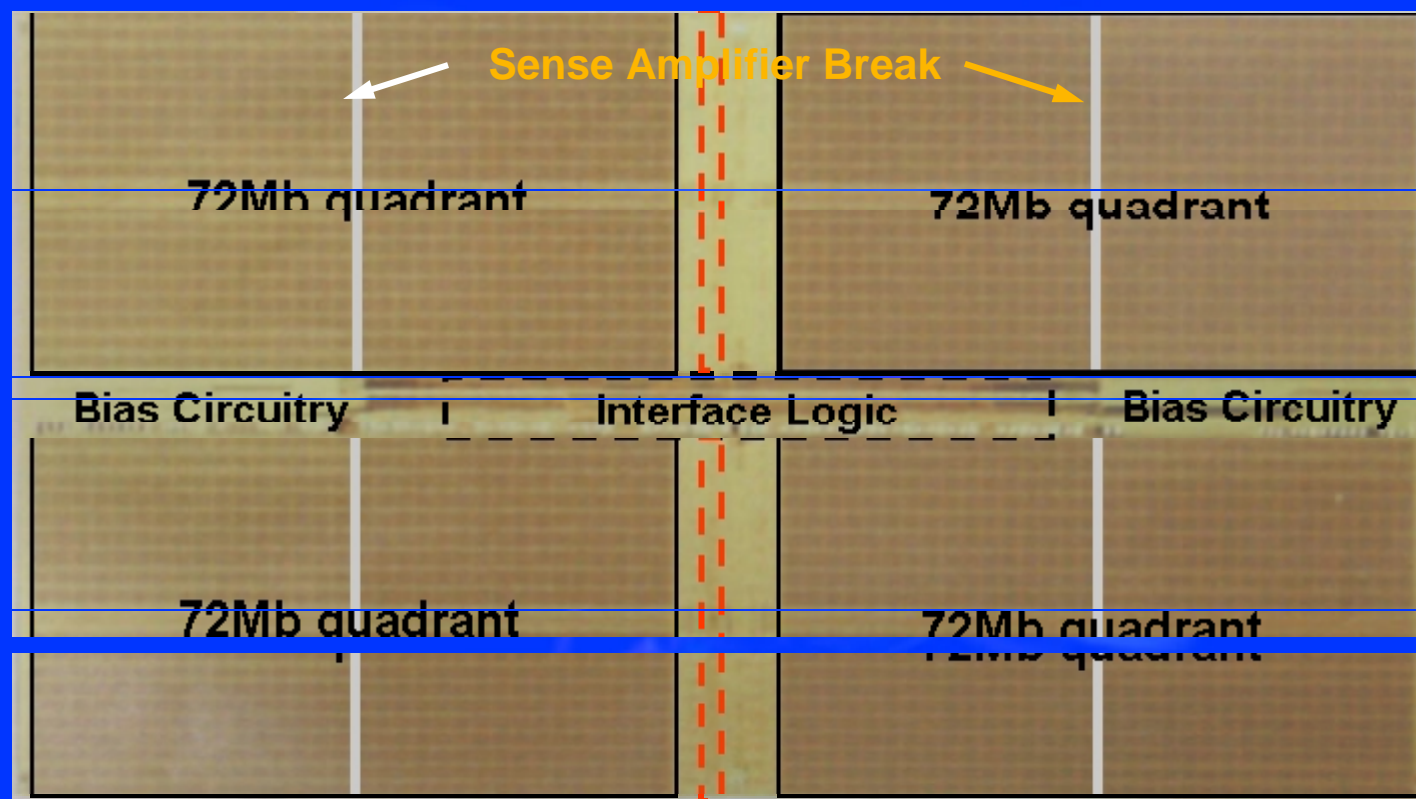
288Mb RDRAM

- Organization:
 - 16M x 18(512R x 128C x 144bit x 32 Bank)
*2 x 16 dependent bank
- Page Size: 2KB
- Frequency: 800/700/600 MHz
- Power Supply: 2.5V +/- 5%
- Power Consumption:
 - Active: 1500mW @800MHz
 - Standby: 300mW
 - Nap: 10mW
- Refresh: 16K cycles/32 msec (multi-Bank refresh)
- Package: 92 pin CSP
- Process Rule :0.175um



Validated and Ramping

TOSHIBA 288Mb RDRAM



Die Size Overhead reduced to under 10%

TOSHIBA
A Passion for Growth

TOSHIBA RIMM (288Mb RDRAM)



RIMM4



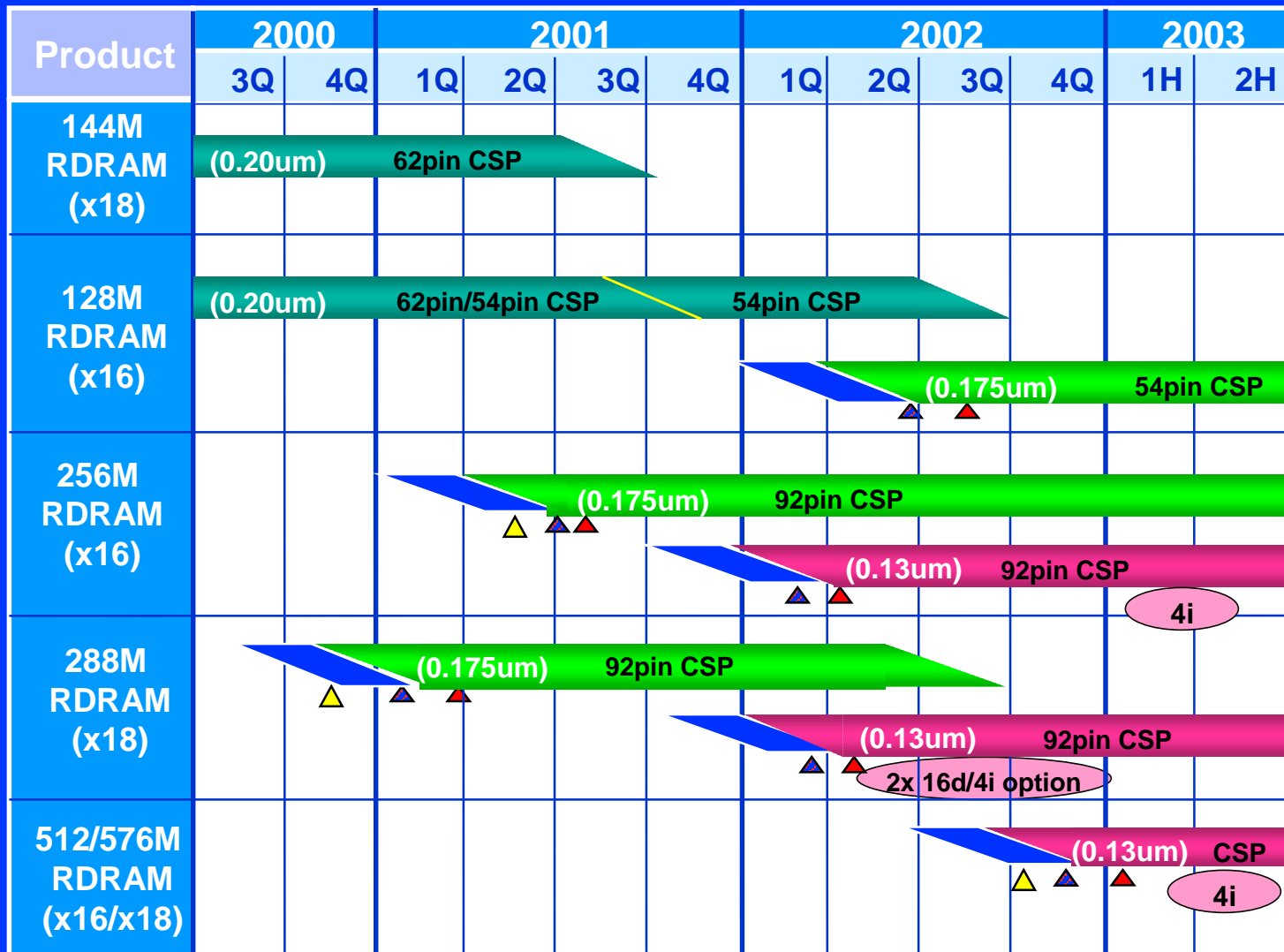
RIMM8



RIMM16
(Double Sided)

Toshiba RDRAM Roadmap

▲ ES ▲ CS ▲ MP — — —



Toshiba RDRAM Schedule

	Technology	Q1'01	Q2	Q3	Q4	Q1'02	Comment
128M	0.20um	MP	MP	MP	*3	*3	See Notes
	0.175um	CS : Q2'02 Convert					Not PC spec
144M	0.20um	MP	MP	MP			
	0.175um	Convert					No plan
256M	0.175um		ES/CS	MP	MP	MP	ES : Jun CS : Jul
	0.13um					ES/CS	4i
288M	0.175um	CS/MP	MP	MP	MP	MP	
	0.13um					ES/CS	2 x 16d / 4i option

Notes:

1. ES/CS = Engineering Sample/Customer Sample ; MP = Mass Production
2. 128M 0.175um version for non PC market
3. 128M 0.20um for PC till Q3'01 and then for non PC from Q4'01

DDR Status

- **Components:**

- 256Mb in production (x4/x8/x16)

- **Modules:**

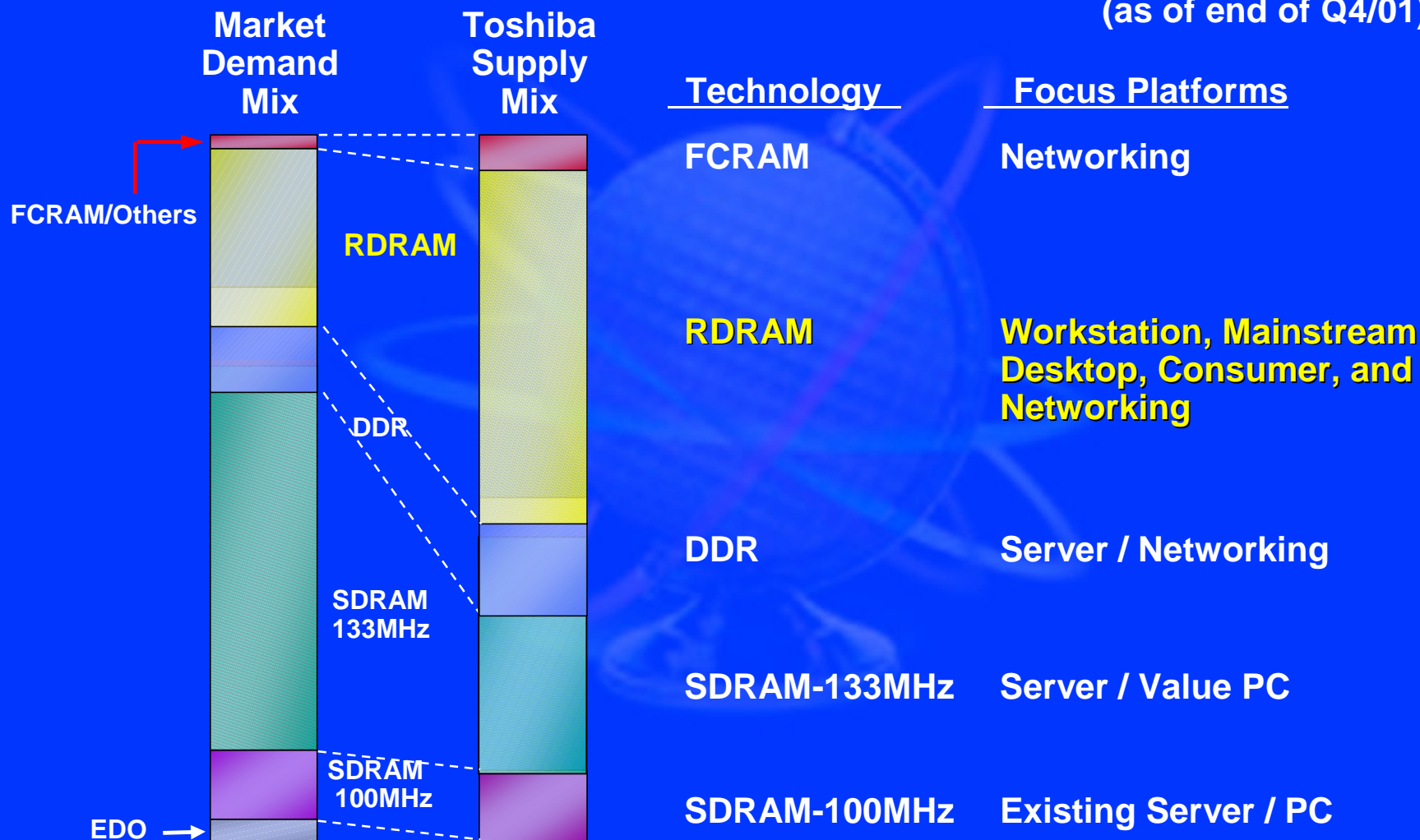
- 256MB to 1GB Registered DIMM
- 128MB to 512MB Unbuffered DIMM

- **Note:**

- Toshiba follows the JEDEC standard.
- Working closely with Intel on DDR JEDEC Spec Addendum.

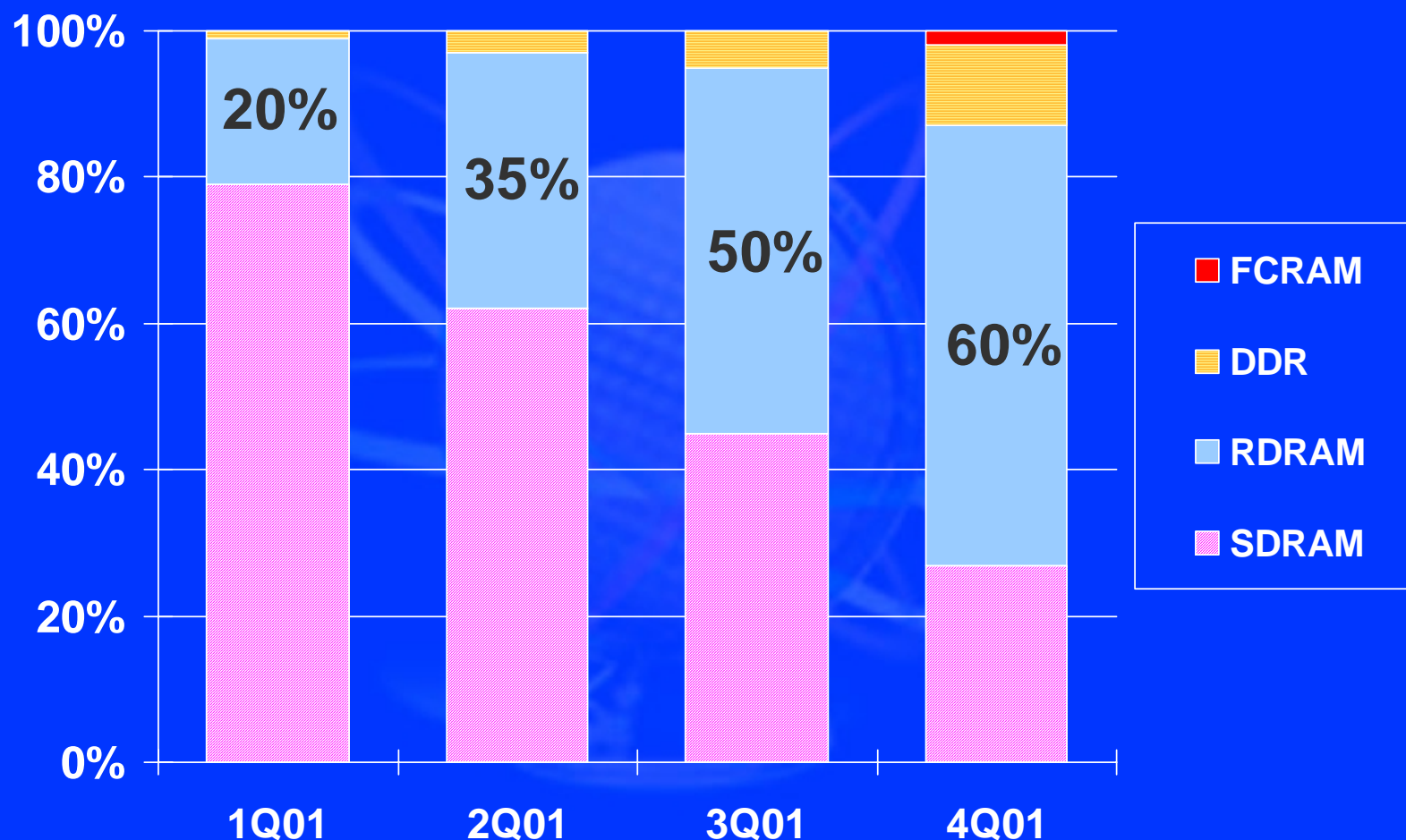
TOSHIBA DRAM Product Mix

(as of end of Q4/01)



◆ Market demand- per Toshiba estimation

Toshiba Production Capacity



RDRAM on an aggressive ramp !

How Toshiba Will Drive down RDRAM Cost

● Device

- Chip shrink (0.20um → 0.175um → **0.13um** → - - -)
- Package Cost reduction (**TOSHIBA BGA** vs uBGA)
- Bank configuration change (2 X 16D → **4i**)

Chip Area Penalty down

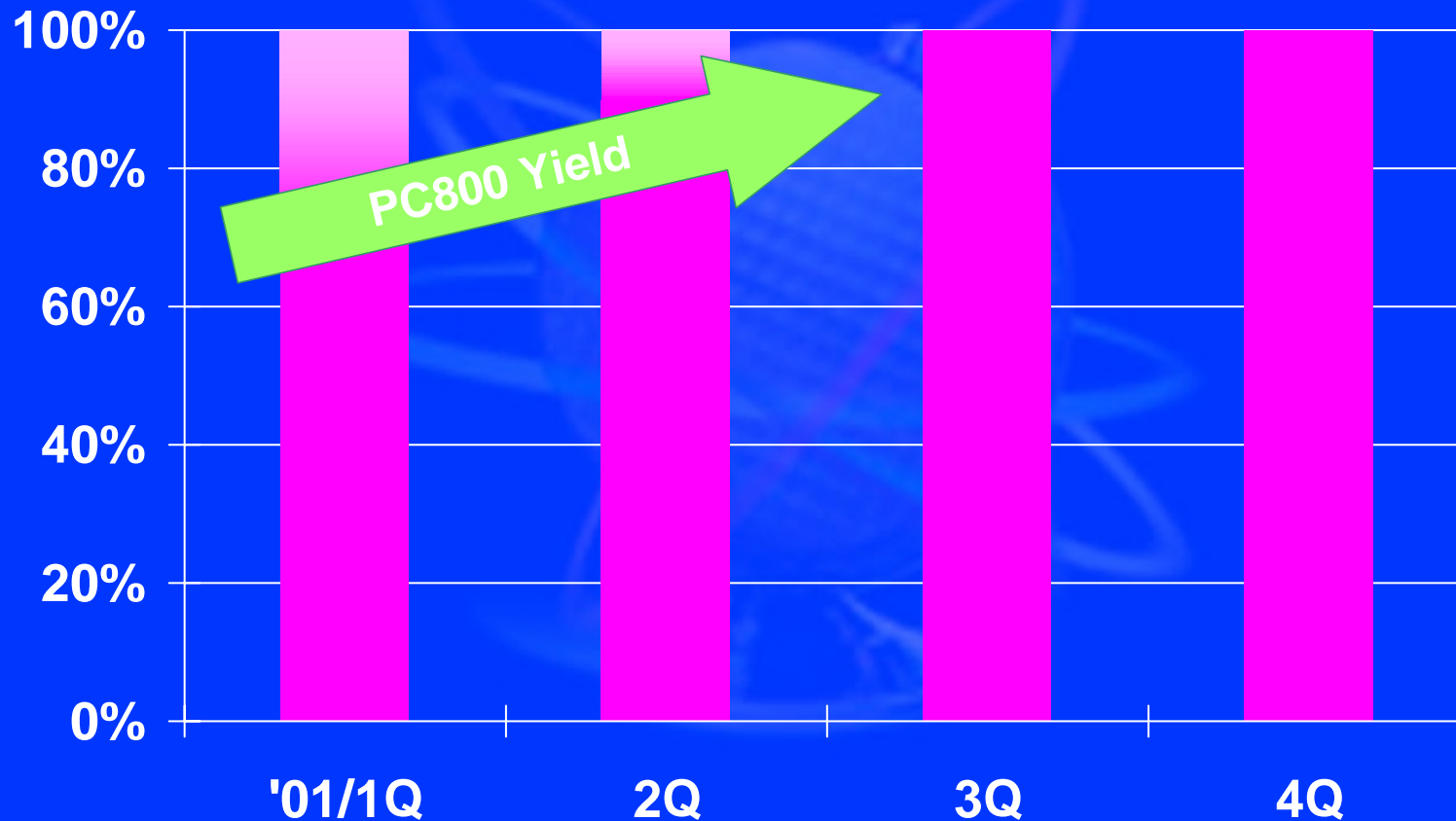
Redundancy Efficiency up

- Test Cost (High Speed Test : 8 DUT → **64 DUT** in parallel)

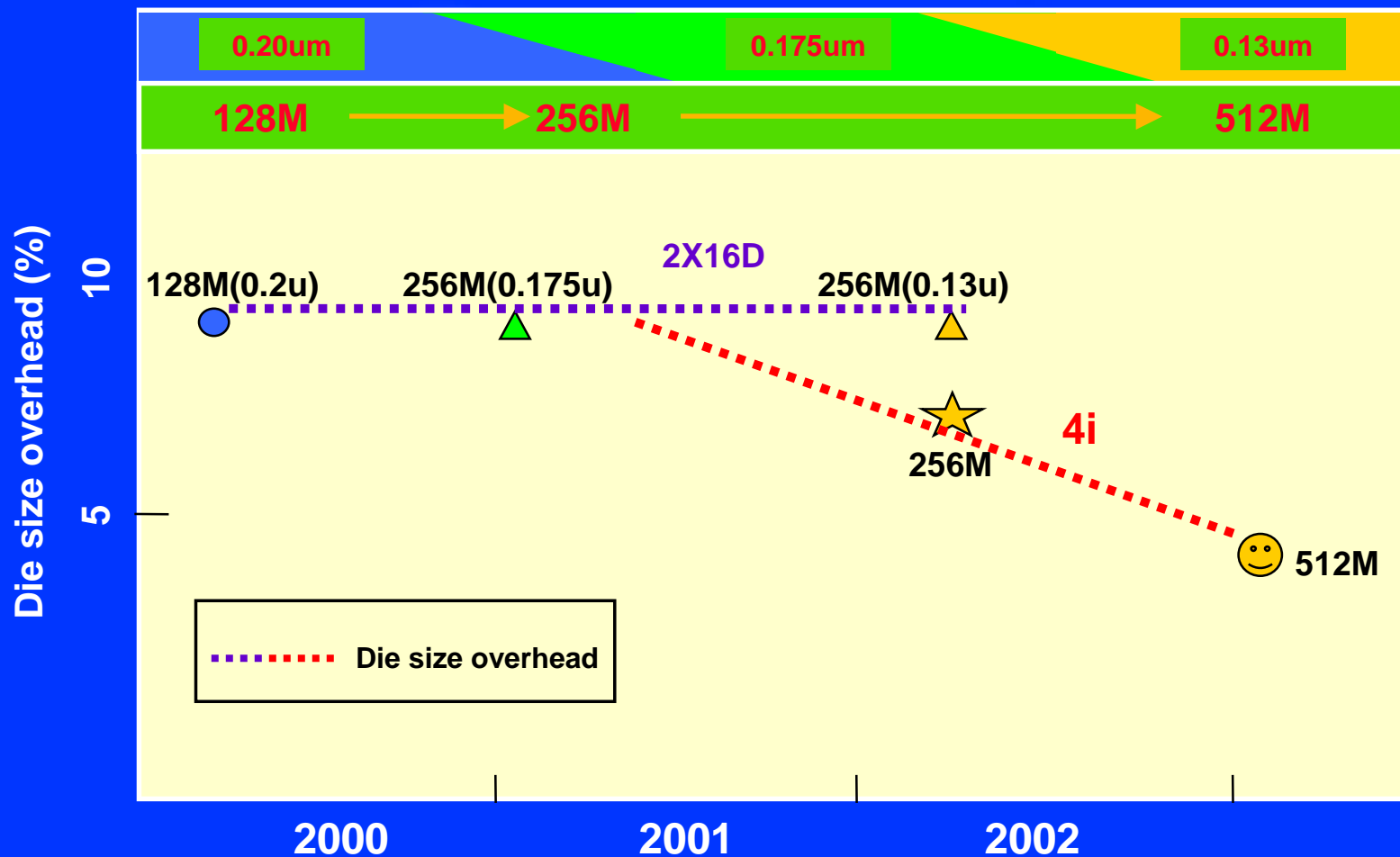
● Module

- Drive down PCB,(8 layer →6 layer) assembly and test costs
- RDRAM granularity allows fewer devices per module
(DIMM vs. RIMM for same data bandwidth)

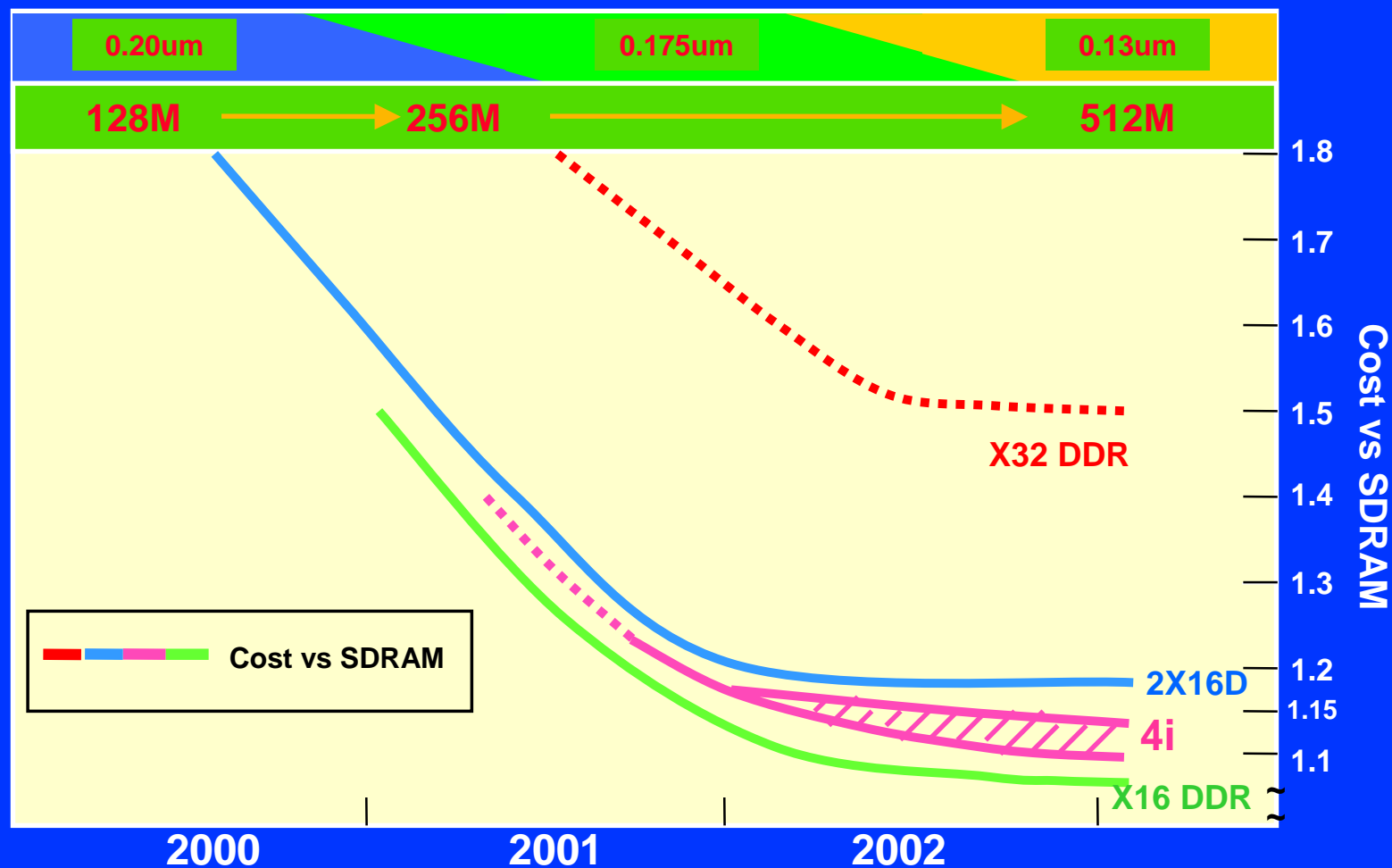
PC800 Yield Improvement



Cost Reduction Plan



Cost Reduction Plan



RIMM Cost Target
'01/End – x1.20 (2x16d)
'02/End – x1.10 (4i)

Summary

- **Full line to support each market segment**
 - RDRAM ... WS / Desktop PC, Digital Consumer
 - DDR ... Server, Networking
 - SDRAM ... Value PC / Mobile PC
 - FCRAM ... Networking
- **Aggressively support RDRAM for Pentium® 4 platforms**
 - Production will increase 5X from 4Q/00 to 4Q/01
 - Continue to pursue cost reduction
 - RDRAM at competitive price for Pentium® 4 ramp

**We support RDRAM
and continue to
build your confidence !**